DOWNLOAD PDF 27 VIRTUAL GAGE WITH INTERNAL MOBILITIES FOR THE VERIFICATION OF FUNCTIONAL SPECIFICATIONS

Chapter 1 : T/T - Wikipedia

We particularly show the immediate way from the expression of a specification to the mathematical method for the verification of a specification and the new functional specification by virtual gauge with internal mobilities.

Knowledge and Information The new gold standard in electrical calibration Since , the A family has set the standard for multifunction calibrator performance in calibration laboratories around the world. Now the time has come to advance this best-in-class calibrator, taking advantage of twenty-first century technology and usability. High performance for the future Like its predecessors, the A calibrates a wide range of digital multimeters, up to long-scale 8. But this new model features improved specifications that will help you increase test uncertainty ratios TURs and increase test confidence. Improved performance specifications for ac voltage, ac current and resistance 6. Metrologists in national laboratories, the military, third party calibration laboratories, and corporate users with high-end workload will value the performance and reliability of the A. Specifications are absolute and include the uncertainty of the calibration standards used. No additional analysis is required. Updated features provide improvements inside and out The A calibrator incorporates the latest technology and usability features. The A keeps many of the front-panel details that characterize its predecessors, while adding a new full color touch screen display to enhance usability and help you calibrate more efficiently. Users enter values via a familiar, calculator-style keyboard, working naturally from left to right. A new graphical user interface features easy-to-read, easy-to-use menus, as well as access to common functions with just the touch of a finger. The touch screen messages are available in your choice of nine languages, including English, French, German, Spanish, Japanese, Chinese, Portuguese, Russian, and Korean. The redesigned front panel features many new improvements. The handles and knob are overmolded for comfort and feel. USB ports are placed both on the front and rear of the unit. Use the port at the front to download internal calibration constants; use the rear port for remote communication with a PCâ€”or choose the LAN, IEEE or serial interfaces. Increased confidence, reduced cost of ownership The A calibrator features Artifact Calibration. Only three artifact standardsâ€”a 10 V dc reference and 1 Ohm and 10 k Ohm resistance referencesâ€”are required to calibrate all ranges and functions to full specifications. Front panel GUI instructions prompt the operator to make connections and inputs each step of the way. The calibrator controls the process, which takes only about an hour, compared to several hours using traditional calibration methods. In addition to saving time and equipment costs, Artifact Calibration can extend time between calibrations of the A to two years before a full verification check by a Fluke Service Center is required. Save time and support costs with Artifact Calibration When Artifact Calibration was first introduced in the Fluke A, customers asked many questions about traceability because they were surprised that you could calibrate so many ranges and functions with only three external standards. However, thanks in part to considerable testing and evaluation by three national laboratories in Europe, Artifact Calibration is fully validated by the metrology community. Today many metrologists rely on Artifact Calibration to maintain their Fluke calibrators at day specifications for up to two years. Significant savings can be realized in calibration costs by only paying for a full verification and shipping to a certified Fluke Service Center every two years. The time savings are also significant, as Artifact Calibration allows the A to remain in service and conducting calibrations when it would otherwise be unavailable due to shipping and service time. Speak to a Fluke Calibration representative today to learn how to embrace this tried and true method of maintaining the traceability of your A. Cal Check monitors performance between calibrations For extra confidence that the A calibrator stays within its specifications between calibrations, the built-in automated Cal Check function checks every range and function against a set of dedicated internal standards to monitor the drift of each. It may surprise many to learn that the internal standards built into every A are the functional and design equivalents of a Fluke B 10 V reference plus two fully characterized metrology-grade resistance standards. These standardsâ€”totally separated from the output circuitryâ€”are not used in normal operation and are provided solely to provide a

check. Improving calibration of 8. The most prevalent long-scale digital multimeters in the world are the Fluke Calibration A and the Agilent A. Due to the high level of accuracy of these two 8. Helping you to sleep well at night It has been become increasingly difficult to meet the industry-recognized test uncertainty ratio TUR of 4: To minimize the chance of approving an out-of-tolerance OOT condition during calibration, the practice of guardbanding is employed. The measured value must now fall within a smaller offset from the nominal value, providing confidence that the actual value is within the new specified band. This gives the metrologist the confidence that the measurement is accurate. High current output to A Paired with a Fluke Calibration A Transconductance Amplifier, the A can output up to A and display the output on the A touch screen display. Operating in closed-loop mode with the A, the A maintains the best current accuracy over the widest range of calibration workload.

DOWNLOAD PDF 27 VIRTUAL GAGE WITH INTERNAL MOBILITIES FOR THE VERIFICATION OF FUNCTIONAL SPECIFICATIONS

Chapter 2 : SerialLite II IP Core User Guide

To ensure a certain level of quality, we define the limits of the geometrical variations of the parts. To do so, we express functional geometrical specifications. In this paper, we present the definition of features used to express the geometrical specifications and the functional expression of the virtual gauge with internal mobilities.

T and T The Soviet T medium tank of the s is considered to have the best balance of firepower F tank gun By the time the T was ready for production, the T had also been modified to fit the same gun. Although the T was superior in most other ways, by this time T production was in full swing and the massive numbers of Ts being built offset any advantage to smaller numbers of a superior design. The T was produced in only small numbers, around 2, being completed during the war. This section needs additional citations for verification. Please help improve this article by adding citations to reliable sources. Unsourced material may be challenged and removed. The main issue was a larger turret ring, which suggested slightly enlarging the hull. This model looked almost identical to the original T, albeit with a much larger gun. It was decided to begin serial production of the new vehicle and the vehicle officially entered service on 29 April It would go into production in Nizhny Tagil in and KharkI v in It has a turret reminiscent of the Ts , with prominent, undercut shot traps. This example has the fender machine gun boxes replaced with fuel tanks. Production of the initial series of Ts began slowly as 1, modifications were made. The Red Army received a tank that was superior to World War II designs and theoretically better than the newest tanks of potential opponents. The serial production version, designated T, differed from the second T prototype. Several changes were made and a new turret was fitted. The new dome-shaped turret with flat sides was inspired by the turret from the IS-3 heavy tank; it is similar to the later T turret but with a distinctive overhang at the rear. It also had a shorter bustle. The fender machine guns were removed in favour of a single bow-mounted machine gun. The tank featured the TDA smoke generating system. A command version was built, the TK komandirskiy , with a second R radio. Morozov was replaced by Kolesnikow, who in turn was replaced by Leonid N. Kartsev in March Originally, this had a small muzzle counter-weight, which was later replaced with a fume extractor. The tank officially entered production in and service in These were not completely successful, so further T development continued to use the D series guns. It never went into production. It entered production in It was decided to create an NBC nuclear, biological, and chemical protection system which would start working 0. The task of creating a basic PAZ Protivoatomnaya Zashchita NBC protection system offering protection against the blast of a nuclear explosion and radioactive particulate filtration, but not against external gamma radiation or gas, [7] was given to the KB design bureau in Kharkiv and was completed in The documentation was sent to Uralvagonzavod. The tank was fitted with the new V cylinder 4-stroke one-chamber Greater engine power was accomplished by increasing the pressure of the fuel delivery and charging degree. The designers planned to introduce a heating system for the engine compartment and MC-1 diesel fuel filter. The engine was to be started pneumatically with the use of an AKS charger and an electric starter. This eliminated the need for the tank to carry a tank filled with air. To allow easier access during maintenance and repairs, it was decided to change hatches over the engine compartment. The original T lacked an antiaircraft machine gun mount. The gunner received a TNP vision device. The tank was supposed to be equipped with the "Rosa" fire protection system. The tank had a thicker turret casting and the improved two-plane gun stabilization system from the TB, as well as night vision fighting equipment. To balance the weight of the new equipment, the armour on the back of the hull was thinned slightly. Despite somewhat thinner frontal turret armour millimetres 7. Heavy tanks soon fell from favour, with only IS-3s produced. The old model of highly mobile medium tanks and heavily armoured heavy tanks was replaced by a new paradigm: Parallel developments in the West would produce similar results. Kartsev combined all the ongoing improvements being offered, or planned, on the T into one design. It suffered a significant lapse in one area: All this additional equipment made it necessary to decrease the ammunition load for the main gun to 37 rounds and eliminate the bow

machine gun. In the beginning of the s, a TK was experimentally fitted with a Uran TV relay apparatus for battlefield surveillance. The tank was fitted with an external camera, the picture from which was relayed to a receiver in a BTRPU command vehicle. There was an observation camera mounted on a folding mast which was in turn mounted on a UAZ 69 car. The range within which the picture could be relayed varied between 10 and 30 kilometres 6. In , a T tank was used to test the "Almaz" TV complex, which was supposed to replace the standard observation devices right after a nuclear explosion or while fording a body of water. There was a camera mounted on the hull for the driver and two cameras mounted on the turret, one for aiming and one for observation, and the picture from the cameras was relayed to two control screens. The tank had the front hull fuel tanks and bow machine gun removed. The cameras allowed battlefield observation and firing during daytime at ranges between 1. Because of the low quality of the equipment, the trials gave negative results. One T tank fitted with this gas turbine engine passed trials but was deemed unsatisfactory and the design did not go into production. The trials found that such gearboxes were prone to frequent breakdowns in tanks. It was fitted with litre tanks filled with flammable liquid instead of the frontal hull fuel tanks. The flamethrower replaced the coaxial machine gun. TO flamethrower tanks were withdrawn from service in The goal was to protect the crew from fast neutrons; adequate protection against gamma radiation was provided by the thick armour and a PAZ basic NBC protection system. The POV plasticized lead antiradiation lining was developed to provide the needed protection. This liner had the added benefit of protecting the crew from fragments of penetrated armour. The hull was lengthened from 6. The hull machine gun was removed, making space for six more main gun rounds. These changes increased the weight of the vehicle to 38 tonnes. In its long service life, the T has been upgraded many times. During production, the TA was frequently modernized. It required a new drive sprocket, with 14 teeth instead of The R radio set was replaced by a R radio set. T and T tanks continued to be upgraded, refitted, and modernized into the s. These improvements make it a potent main battle tank MBT for the low-end budget, even to this day. One of these upgrade packages was produced by Cadillac Gage Textron and a prototype named the Jaguar was produced. The Jaguar looked quite different from its predecessors. A newly designed turret was formed by flat armour plates installed at different angles. The hull top was new. The engine compartment and fuel tanks on the shelves over the tracks were armour-protected. A Marconi fire control system which was originally developed for the American light tank Stingray was fitted. In , two Jaguar tanks were manufactured. The chassis were provided by PRC, while the hull tops, turrets and powerplants were manufactured by Cadillac Gage Textron. After further modifications and trials it was sent into mass production and received the designation Ramses II. As late as , Ukrainian companies were reportedly developing T main battle tank upgrades targeting the export market. The T and T have a cabin layout shared with many post-World War II tanks, with the fighting compartment in the front, engine compartment in the rear, and a dome-shaped turret in the center of the hull. The commander is seated on the left, with the gunner to his front and the loader on the right. Engine exhaust is on the left fender. There is a prominent gap between the first and second road wheel pairs, a distinguishing feature from the T, which has progressively larger spaces between road wheels towards the rear. The T and T tanks are outwardly very similar and difficult to distinguish visually. They are very simple to operate compared to Western tanks, and do not require a high level of training or education in their crew members. The tanks have good mobility thanks to their relatively light weight which permits easy transport by rail or flatbed truck and allows crossing of lighter bridges , wide tracks which give lower ground pressure and hence good mobility on soft ground , a good cold-weather start-up system and a snorkel that allows river crossings. An abandoned Iraqi Army T tank lies among the wreckage of many other Iraqi vehicles, such as trucks, cars and buses, somewhere along the Highway of Death in April According to Zaloga, "By the standards of the s, the T was an excellent tank combining lethal firepower, excellent armor protection and good reliability" [15] while remaining a significantly smaller and lighter tank than its NATO contemporariesâ€”the US M48 Patton tank and the British Centurion tank. Small size is achieved at the expense of interior space and ergonomics, which causes practical difficulties, as it constrains the physical movements of the crew and slows operation of controls and equipment. This is a

common trait of most Soviet tanks and hence height limits were set for certain tank crew positions in the Soviet Army, whereas other armies may not include crew member height limits as standards. As in most tanks of that generation , the internal ammunition supply is not shielded, increasing the risk that any enemy penetration of the fighting compartment could cause a catastrophic secondary explosion. All of these problems were corrected in the otherwise largely identical T tank.

DOWNLOAD PDF 27 VIRTUAL GAGE WITH INTERNAL MOBILITIES FOR THE VERIFICATION OF FUNCTIONAL SPECIFICATIONS

Chapter 3 : USB1 - Static scheduling of test cases - Google Patents

Inspection and Gaging Tools Screw pitch gages 26 February 6, Template 27 February 6, MMC can be checked with a functional gage as.

Overview[edit] Although testing can determine the correctness of software under the assumption of some specific hypotheses see hierarchy of testing difficulty below , testing cannot identify all the defects within software. These oracles may include but are not limited to specifications, contracts , [3] comparable products, past versions of the same product, inferences about intended or expected purpose, user or customer expectations, relevant standards, applicable laws, or other criteria. A primary purpose of testing is to detect software failures so that defects may be discovered and corrected. Testing cannot establish that a product functions properly under all conditions, but only that it does not function properly under specific conditions. In the current culture of software development, a testing organization may be separate from the development team. There are various roles for testing team members. Information derived from software testing may be used to correct the process by which software is developed. For example, the audience for video game software is completely different from banking software. Therefore, when an organization develops or otherwise invests in a software product, it can assess whether the software product will be acceptable to its end users, its target audience, its purchasers and other stakeholders. Software testing aids the process of attempting to make this assessment. Defects and failures[edit] Not all software defects are caused by coding errors. One common source of expensive defects is requirement gaps, e. Software faults occur through the following processes. A programmer makes an error mistake , which results in a defect fault, bug in the software source code. If this defect is executed, in certain situations the system will produce wrong results, causing a failure. For example, defects in dead code will never result in failures. A defect can turn into a failure when the environment is changed. Examples of these changes in environment include the software being run on a new computer hardware platform, alterations in source data , or interacting with different software. Input combinations and preconditions[edit] A fundamental problem with software testing is that testing under all combinations of inputs and preconditions initial state is not feasible, even with a simple product. More significantly, non-functional dimensions of quality how it is supposed to be versus what it is supposed to do â€" usability , scalability , performance , compatibility , reliability â€"can be highly subjective; something that constitutes sufficient value to one person may be intolerable to another. Combinatorial test design enables users to get greater test coverage with fewer tests. Whether they are looking for speed or test depth, they can use combinatorial test design methods to build structured variation into their test cases. More than a third of this cost could be avoided, if better software testing was performed. Until the s, the term "software tester" was used generally, but later it was also seen as a separate profession. Regarding the periods and the different goals in software testing, [11] different roles have been established, such as test manager, test lead, test analyst, test designer, tester, automation developer, and test administrator. Software testing can also be performed by non-dedicated software testers. Testing approach[edit] Static vs. Reviews , walkthroughs , or inspections are referred to as static testing, whereas actually executing programmed code with a given set of test cases is referred to as dynamic testing. Dynamic testing takes place when the program itself is run. These two approaches are used to describe the point of view that the tester takes when designing test cases. A hybrid approach called grey-box testing may also be applied to software testing methodology. White-box testing White-box testing also known as clear box testing, glass box testing, transparent box testing, and structural testing verifies the internal structures or workings of a program, as opposed to the functionality exposed to the end-user. In white-box testing, an internal perspective of the system the source code , as well as programming skills, are used to design test cases. The tester chooses inputs to exercise paths through the code and determine the appropriate outputs. While white-box testing can be applied at the unit , integration , and system levels of the software testing process, it is usually done at the unit level. Though this method of test design can uncover

many errors or problems, it might not detect unimplemented parts of the specification or missing requirements. Techniques used in white-box testing include: This allows the software team to examine parts of a system that are rarely tested and ensures that the most important function points have been tested. This is helpful in ensuring correct functionality, but not sufficient since the same code may process different inputs correctly or incorrectly. Pseudo-tested functions and methods are those that are covered but not specified it is possible to remove their body without breaking any test case. Black-box testing Black box diagram Black-box testing also known as functional testing treats the software as a "black box", examining functionality without any knowledge of internal implementation, without seeing the source code. The testers are only aware of what the software is supposed to do, not how it does it. Test cases are built around specifications and requirements, i. It uses external descriptions of the software, including specifications, requirements, and designs to derive test cases. These tests can be functional or non-functional , though usually functional. Specification-based testing may be necessary to assure correct functionality, but it is insufficient to guard against complex or high-risk situations. Whatever biases the programmers may have had, the tester likely has a different set and may emphasize different areas of functionality. On the other hand, black-box testing has been said to be "like a walk in a dark labyrinth without a flashlight. This method of test can be applied to all levels of software testing: Component interface testing Component interface testing is a variation of black-box testing , with the focus on the data values beyond just the related actions of a subsystem component. One option for interface testing is to keep a separate log file of data items being passed, often with a timestamp logged to allow analysis of thousands of cases of data passed between units for days or weeks. Tests can include checking the handling of some extreme data values while other interface variables are passed as normal values. Visual testing[edit] The aim of visual testing is to provide developers with the ability to examine what was happening at the point of software failure by presenting the data in such a way that the developer can easily find the information she or he requires, and the information is expressed clearly. Visual testing, therefore, requires the recording of the entire test process â€” capturing everything that occurs on the test system in video format. Output videos are supplemented by real-time tester input via picture-in-a-picture webcam and audio commentary from microphones. Visual testing provides a number of advantages. The quality of communication is increased drastically because testers can show the problem and the events leading up to it to the developer as opposed to just describing it and the need to replicate test failures will cease to exist in many cases. The developer will have all the evidence he or she requires of a test failure and can instead focus on the cause of the fault and how it should be fixed. Ad hoc testing and exploratory testing are important methodologies for checking software integrity, because they require less preparation time to implement, while the important bugs can be found quickly.

Chapter 4 : Table of contents for Library of Congress control number

the interface gauge/part defining the relative position between the ideal surfaces of the gauge and the actual surfaces of the part, (ii) the gauge structure modeling the environment of the part, the environment being composed of the parts of the mechanism and of their mobilities, (iii) the functional characterisation by geometrical characteristics directly related to the function of the mechanism.

The entire disclosure of provisional application No. It is now notoriously well-known that a vast array of consumer products, especially those products in the area of telecommunications and computerized devices including personal computers , are based on ICs, such as central processing units CPUs , microprocessors, and, of course, digital memory devices of many sorts. In the art of IC design and manufacturing, ongoing research and development in a highly competitive environment is conducted to produce new and better devices, which are manufactured by usually well-know techniques involving many ways of treating semiconductor materials wafers , applying thin-film materials, patterning, and selectively removing materials to create highly concentrated matrices of interconnected semiconductor elements, such as transistors, providing, in the end, minute, complex circuitry to perform specific tasks of computation and logic with almost unbelievable rapidity and reliability. Also typically, in the manufacturing process, many ICs are formed on a single wafer. When developmental engineers conceive a new chip, it is of course necessary to lay out all of the circuits that will accomplish the purposes, which amounts to placing all transistors, resistors, and other devices, and plotting the interconnections that complete the circuitry. In the very early days of chip design this was a relatively straightforward process, at least a lot more straightforward than it is today. The trend in design, however, has always quite naturally been to faster and faster operation clock speed , higher and higher density area needed for circuitry , and lower power consumption to attain maximum computing or storage power in the least possible space. The speed motivation is obvious. Part of the density motivation is dictated by space and volume requirements in product design, and part by cost considerations. More good chips per wafer drives the cost per part down. As need for density and speed steadily increase, new challenges arise in IC design. For example, specific manufacturing techniques, lithography for example, are always limited to such as minimum spacing of elements on a chip, line width in interconnects, and the like, and to achieve higher density it is often necessary to invent new processing techniques or improvements in older techniques. Likewise, even though higher density has a usually beneficial effect on speed capability devices are connected closer together , allowing higher operating rate clock speed , there are always limitations associated with device structure, materials, and the like, to speed as well, and achieving higher and higher speed involves new inventions and discoveries in materials, combinations of materials, structures of devices, and so on. It therefore becomes apparent that a circuit diagram is only a starting point in a new IC design, even though massive computing engines are needed even for this seminal part of a design. Given stringent requirements for a new design for speed, density, and power consumption, development engineers have to pick very carefully among many alternatives for materials, processes, film characteristics and thicknesses, interconnection alternatives, and much more; and the selections one makes almost always influence other possible selections and decisions, as all are intimately related. Integrated circuit designers are therefore under tremendous pressure to design complex chips to meet design and marketing requirements. The design of complex multi-million-transistor chips requires the pervasive use of electronic design automation EDA software tools. These tools are used to take high-level descriptions of designs in languages that are very similar to programming languages and yield, through a series of complicated steps, the final mask for a chip. To counter the risk of designs not converging on requirements, engineers use virtual prototyping tools, a type of EDA tool, to estimate downstream chip implementation characteristics speed, area, power from early design descriptions. The intent is to get an early gauge of design feasibility. Virtual prototyping tools have garnered significant interest in the design community, and virtual prototyping is among the fastest growing of EDA

market segments. Virtual prototyping tools arguably provide reasonable estimates of delays along timing paths on a chip. The feasibility of a design, however, hinges on whether these delays are actually within acceptable bounds. Without good constraints on the permissible delays for the millions of timing paths on a chip, virtual prototyping tools are insufficient to gauge actual design feasibility. This severely impacts ability of such tools to generate low-cost, low-power implementations that meet performance requirements without requiring design iterations. What is clearly needed is a tool that starts with the fundamental speed performance requirements for an IC to be designed, i. Such a tool could generate golden timing constraints that must be obeyed for the finished chip to operate at its intended clock speed. Fundamental to the golden timing constraints for a chip is that they describe not only the bounds on path delays that are established by the clock requirements of a chip, but that they also identify paths on a chip where clock requirements are relaxed. The automatic identification of the exceptions to single-cycle clocking is fundamental to the generation of the golden timing constraints for a chip. The use of the golden constraints could, because of the automatically generated exceptions to clock requirements, then empower chip design without expensive and time consuming iterations, while also yielding chips that consume less area, less power, or, if required, run faster than was thought possible. A unique and innovative software system, called Focus by the inventors, for developing such golden timing constraints in IC design is taught in enabling detail in the descriptions of preferred embodiments below. In preferred embodiments, the processing unit, in determining the timing constraints, determines exceptions to single-cycle clocking for the proposed IC design. Further, in a preferred embodiment the exceptions include false paths and multi-cycle paths. In one aspect of the invention the first and second inputs and output timing constraints may be for an individual functional block on an IC instead of for the entire IC. In another aspect the first and second inputs and output timing constraints may be for paths between functional blocks on an IC. In the latter case the results may be used to partition overall IC timing requirements into block timing budgets. In other embodiments the first input may be derived from a. In one embodiment a facility is provided for a user to manually refine an automatically-generated model by adding functional detail. In various embodiments, as a part of clock specification, users may define the clocks, their periods, their phase shifts relative to a reference clock, and the nets on the design to which a clock is applied. In another aspect of the invention a method for guiding an implementation phase for a proposed IC design is provided, comprising the steps of a providing to a processing unit as a first input a synthesizable description of the proposed IC; b providing as a second input to the processing unit clock specification for the proposed IC; and c using the first and the second inputs by the processing unit to determine therefrom, as an output, a set of timing constraints to guide implementation of the proposed IC design. In preferred embodiments of the method, in step c , the processing unit, in determining the timing constraints, determines exceptions to single-cycle clocking for the proposed IC design. The exceptions may include false paths and multi-cycle paths. In some cases the first and second inputs and output timing constraints may be for an individual functional block on an IC instead of for the entire IC. Also in some cases the first and second inputs and output timing constraints are for interaction paths between functional blocks on an IC, and may be used to partition overall IC timing requirements into block timing budgets. Further, there may be a facility provided for a user to manually refine an automatically-generated model by adding functional detail. In other embodiments of the present invention, as part of the clock specification, users define the clocks, their periods, their phase shifts relative to a reference clock, and the nets on the design to which a clock is applied. The Focus system, as summarized above, provides significant advantages in IC design, by providing: A reduction in the risk of design failures by providing engineers an early understanding of the precise challenges they face in realizing a design. By providing virtual-prototyping tools with golden timing constraints, the Focus system empowers the tools to create more realistic block timing budgets. Correct block implementation constraints, in turn, reduce the risk of design iterations. A reduction in the cost and power consumption of a design. By generating timing constraints that do not over-constrain a design, the Focus system allows block implementation tools to generate circuits that consume as little area and power as possible, while meeting performance objectives.

Reduction in IC area typically translates to a reduction in unit costs. Reduction in power consumption is crucial for several consumer products. A reduction in IC design time by automating a task that is central to IC design. Engineers conventionally specify timing constraints in an ad-hoc and continually evolving manner. As timing problems are uncovered, and most of them tend be uncovered late in the implementation flow, exceptions to single-cycle clocking are inserted. All of this takes time, is error-prone and is the source of much anxiety during IC sign-off. The Focus system empowers an RTL-handoff-based design flow. With the Focus system, system design houses are able to describe the design they want to implement and hand this design, along with its constraints, to a semiconductor vendor that will take responsibility for implementing the design to meet requirements. Semiconductor vendors typically prefer RTL handoff because it allows them to take responsibility for a greater portion of the design flow. System design houses prefer RTL handoff because it allows them to focus on their core competency, which is the design of compelling products. In embodiments of the invention described in enabling detail below, for the first time a system is provided that allows users to identify false and multi-cycle paths ahead of implementation of a proposed design, and to use timing constraints determined therefrom in implementing the proposed design. It is well-known that there are, broadly speaking, two historically distinct stages in the creation of a new IC: The system of the invention, termed Focus by the inventors, links the two stages for the first time by establishing constraints imposed on the implementation stage by facts and characteristics of the design stage. It is well-known that development engineers constrain the delays on the timing paths of a proposed IC based on the speed at which they intend to clock the IC. The engineers specify the clocks on their design and every timing path on the IC is required to have a delay less than the clock cycle. Known IC implementation tools strive to reduce path delays so that they are less than a clock cycle. There are, however, large numbers of timing paths in almost any design that are not relevant, that is, the functionality of the IC is such that the delay on these paths does not matter. These paths are typically termed false paths, although they are false only in terms of the fact that the delay does not matter. There are also typically a significant number of timing paths on a proposed IC wherein, by design, engineers provide extra time to perform complex operations. These paths are termed multi-cycle paths. False and multi-cycle paths are collectively referred to as exceptions to single-cycle clocking. The present inventors have determined that the critical timing constraints for an IC are defined by the clocks and exceptions to single-cycle clocking. At the time of filing the present patent application, it is known that engineers do not typically specify exceptions to clocking at the start of design flow. Instead, the engineers respond to timing problems reported by conventional IC implementation tools and, based on communication between design and verification engineers, establish whether a timing problem is real or needs to be handled by adding a timing exception to the constraint file for a design. This conventional process is an error-prone, time-consuming, process that continues throughout IC implementation flow, and compounds errors in the overall process. The Focus system, as shown by the flow of FIG. Without requiring any other information, the Focus system generates exceptions false paths, multi-cycle paths to single-cycle clocking. By automatically identifying exceptions to clock requirements, the Focus system relaxes the timing goals that an IC implementation must to obey. These exceptions and the user-provided clock definitions constitute golden timing constraints for an IC under consideration. The Focus system is applicable as well for both synchronous and asynchronous designs. Focus is also applicable for the design of large and complex SoCs that contain 10 million or more gates and run at clock speeds in excess of megahertz MHz , as well as for the design of FPGAs containing less than a million gates that run at speeds up to MHz or more. Further, the Focus system may be used to constrain and drive the implementation of individual blocks within an IC, as well as the entire IC. Considering the full IC, the Focus system is used to generate the golden timing constraints that constrain the interaction among blocks on the IC. These constraints are then imported by such as virtual prototyping tools, and used to partition overall IC timing requirements into block timing budgets that establish when information is available at the inputs of a block and when information must be available at the outputs of a block. Considering IC block implementation flow, the Focus system generates the golden timing constraints for the internal implementation

of a block. The Focus system in preferred embodiments is plug-and-play in existing design flow. Therefore engineers do not need to alter the way they do design, and they need to provide only minimal new information to the Focus system. The information the Focus system requires, which is substantially synthesizable design descriptions and clock specifications, is already at hand at the start of IC implementation flow. The information the Focus system generates is generated in a standard form SDC that is accepted across the industry by major EDA players and start-ups alike. The Focus system does not replace existing design tools, it simply makes them more effective. The synthesizable description for a design is provided as input to Focus in Verilog or VHDL format, both of which are well-known to the skilled artisan. All conventional synthesizable constructs in these languages are supported by the Focus system. Information for blocks on an IC design that do not have synthesizable descriptions, such as for external hard IP blocks, embedded memory, or user-instantiated library cells, for example, is provided as input to the Focus system using one of two approaches: This model describes black-box timing relationships between pins on the block. Users can refine this auto-generated model manually by adding functional detail. This interface-logic model, generated in Verilog or VHDL format, may be used as input to Focus in lieu of the full synthesizable description for a block. The constraints for a design can be generated using either a flat or hierarchical methodology.

DOWNLOAD PDF 27 VIRTUAL GAGE WITH INTERNAL MOBILITIES FOR THE VERIFICATION OF FUNCTIONAL SPECIFICATIONS

Chapter 5 : EUR-Lex - L - EN - EUR-Lex

Bibliographic record and links to related information available from the Library of Congress calendrierdelascience.com: Electronic data is machine generated. May be incomplete or contain other coding.

A static scheduler is used to schedule the entire verification test of an integrated circuit in advance. The static scheduler is used in conjunction with a hardware description language HDL circuit design, a virtual test bench, and simulation software. The static scheduler is configured to assign test events to resources, or functional units, of the integrated circuit design. Events for a resource are assigned to available time slots, or cycles. During event scheduling, the static scheduler is configured to ensure that there are no resource conflicts for a given time slot. By scheduling all test events in advance, pitfalls associated with dynamic scheduling may be avoided, such as those associated with the use of semaphores. By avoiding the use of semaphores, complex test scenarios and boundary conditions may be more fully exercised, as resources will not be locked. This may allow a more thorough verification of an integrated circuit design. Field of the Invention This invention relates to design verification of integrated circuits, and more specifically, to the scheduling of specific test events. Description of the Related Art A common method of designing integrated circuits involves the use of a hardware description language, or HDL. Once an initial design is completed, simulations may be run to verify the behavior of the circuit. If the circuit does not meet behavioral specifications, the design may be modified to allow the circuit to perform its desired function. The ability to verify a design at a simulation level prior to constructing working hardware models may allow for significant cost savings in the overall design process. In order to test a circuit during the design phase, many designers use a virtual test bench. A virtual test bench is a software package that allows a user to construct a virtual environment in which the simulation will take place. This virtual environment may include input stimuli and models of external devices, as well as a model of the device under test DUT. In some cases, the virtual test bench is a component of the hardware description language used to design the circuit, while a separate software package is used to effect the simulation. For example, the hardware description language Verilog may use a software package known as Verilog-XL. The Verilog-XL package is used to simulate the virtual test bench environment specified by the Verilog hardware description language. For a given simulation, a user may describe a specific set of events which are to occur. These events will employ the various resources of the DUT in order to verify their function. Typically, the scheduling of the specified events occurs dynamically during the actual simulation. One hazard of using dynamic scheduling is the possibility of resource conflicts. Such resource conflicts may be prevented by the use of semaphores. A semaphore will lock the resource in use, preventing its use by other resources at a given time, as well as preventing the simulation from attempting to use the resource for multiple events simultaneously. Although semaphores may simplify the dynamic scheduling of events in a simulation, there may be overhead associated with their use. Using a semaphore to lock a resource during a given test may not allow the full functionality of the given resource to be properly tested. This can result in an incomplete test of the FIFO memory. As an alternative, the simulation may be accomplished without the use of semaphores, but this may lead to resource conflicts that may potentially result in the performance of illegal operations. Because of the limitations of dynamic scheduling, it is possible that some complex test scenarios will not be simulated during a given test. In order to verify the full functionality of a given resource, multiple simulations may need to be performed. In some cases, it may be impossible, even with multiple simulations, to verify the full functionality of a resource using dynamic scheduling. In one embodiment, a static scheduler is used to create a plurality of arrays, each array including a plurality of time slots. Events are then scheduled into available time slots. Each of these events may be defined as the allocation of a specific resource during the given time slot of the simulation, with a predefined action taking place on the resource. For example, an event may be defined as driving a data packet to an input port during a specified clock cycle. When assigning events to an array of time slots, the scheduler will check each of the events previously assigned to the plurality of arrays for resource

conflicts. When a given resource is free for a given time slot, an event may then be assigned to that resource in that time slot. The scheduler will continue to assign events to time slots in the various arrays until the specified events for each resource are allocated to time slots. In one embodiment, the device under test DUT is an integrated circuit design created using a hardware description language HDL. The HDL software package includes a virtual test bench that may be used to create a virtual test environment for the DUT. The virtual test environment may include information about the data to be driven to and from the DUT, interconnecting components, and timing. The virtual test bench may also be used to define boundary conditions for the DUT. A simulation software package may then be used to create a verification test for the integrated circuit design based on information from hardware description and the virtual test bench. The simulation software package implements a programming language, which is used to program the static scheduler. The static scheduler may be used to schedule test events in prior to performing the simulation, ensuring that there are no resource conflicts in anytime slots of the simulation. When the desired test events have been scheduled, the simulation software may then perform the verification test on the integrated circuit design. Thus, in various embodiments, the system and method for static scheduling of test cases may allow for greater control of verification tests for integrated circuit designs. Since semaphores are not used as they are when dynamic scheduling is performed , resources i. Boundary conditions, such as simultaneous reading and writing of a first-in first-out FIFO memory may be more thoroughly tested since resources such as these will not be locked by a semaphore when a single event is applied to them. Static scheduling may allow for more complex test scenarios, thereby yielding a more thorough verification test for an integrated circuit design. While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and description thereto are not intended to limit the invention to the particular form disclosed, but, on the contrary, the invention is to cover all modifications, equivalents, and alternatives falling with the spirit and scoped of the present invention as defined be the appended claims. In this embodiment, verification test system is configured to create and run tests of integrated circuit designs prior to actual fabrication of the circuit. Verification test system includes three main components: Typically, HDL will be part of a software package, such as Verilog. Other embodiments using different HDL software packages are contemplated. Using HDL , a circuit designer may input an integrated circuit design by creating a source code file. The source code file may be created based on integrated circuit design specifications decided upon before commencing the actual design. The source code file typically describes the functional behavior of the circuit, and may describe desired electrical characteristics as well. The behavior described in the source code file may be a simple as that of basic logic function, such as an inverter, an AND gate, an OR gate, or other function. Conversely, a source code file created with HDL may describe behavior for very complex functions, such as an execution unit of a microprocessor or a functional unit of an application specific integrated circuit ASIC. It should also be noted that HDL may describe the behavior of either analog or digital circuits, or hybrids thereof. Synthesis is the process of creating the actual physical circuit design. In order to begin synthesis, the designer may specify various constraints such as circuit area, electrical characteristics, clocking periods, and so on. With these constraints specified, the synthesis is begun. If successful, a physical design of the circuit is created which can be used to create working models. In the embodiment shown, the software package for HDL includes virtual test bench Other embodiments in which the virtual test bench may be a stand-alone application or part of another application are contemplated. Virtual test bench is used to create a virtual test environment in which the integrated circuit design will be tested. The environment created using virtual test bench may include virtual models of external devices to which the integrated circuit is to be coupled, such as other integrated circuits. Discrete components, such as resistors or capacitors, as well as system buses may be modeled as well. Test environment specifications are provided as inputs to virtual test bench These specifications may define exactly which types of devices, components, and buses are to be modeled as coupled to the integrated circuit design. The test environment specifications may also allow the virtual test bench to add other parameters to

the virtual test environment, such as timing intervals or electrical specifications. In the embodiment shown, in which virtual test bench is a component of the software package for HDL , the virtual test environment may be described using the same hardware description language as the integrated circuit design. Simulation software is a software package is configured to create and perform the actual verification test of the integrated circuit design. Simulation software is configured to receive HDL circuit design and virtual test environment as inputs. Also received by simulation software are test event specifications, which specify the specific events of the test which are to take place. Typically, an event is defined as an action taking place on a resource of the integrated circuit design. For example, reading the contents of a register may be defined as an event, as well as writing to an on-board cache memory. Included in this embodiment of simulation software is static scheduler Static scheduler is configured to schedule events to resources, ensuring that there are no resource conflicts. Static scheduler creates a plurality of arrays which define the schedule of events for the verification test. Arrays may be organized in a number of different ways. For example, in one embodiment, a plurality of one-dimensional arrays corresponding to resources of the integrated circuit may be defined. Each element of the array may be a time slot, or clock cycle, to which events for that resource are defined. Initially, all time slots will be empty. Static scheduler will begin by assigning an event to a resource in an open time slot. With each subsequent assignment, static scheduler will search all arrays for resource conflicts prior to assigning an event to a resource. For example, if the static scheduler intends to assign an event such as the driving of a data packet to a port from a source external to the device under test DUT , it may first check all other arrays in order to ensure that no other port or external source is attempting to simultaneously drive data to the same port. This process repeats until assignment of events to resources is complete. By creating arrays in this manner, the entire verification test may be scheduled prior to its actual execution, which may allow the avoidance of the pitfalls associated with dynamic scheduling, as previously described. The final output of the simulation software, following the scheduling of events, is verification test Verification test is configured to test the integrated circuit design and compare the results gathered during the test with expected results. Testing of the integrated circuit design may occur either prior to or following design synthesis. In many situations, testing will occur both prior to and following synthesis. For those tests which occur following synthesis, circuit-level testing may be performed in addition to functional level testing. Circuit level testing may allow the verification of desired electrical characteristics.

DOWNLOAD PDF 27 VIRTUAL GAGE WITH INTERNAL MOBILITIES FOR THE VERIFICATION OF FUNCTIONAL SPECIFICATIONS

Chapter 6 : USB2 - Automated approach to constraint generation in IC design - Google Patents

The Maximum Material and the Least Material Requirements are verified by the use of virtual gauges with internal mobilities [5].

True Position Special Note: We explain why it is much better to use a Position tolerance and Basic Dimensions over locating your feature with a coordinate dimension system. However, since this is such a useful symbol, we will continue to add content and examples for other uses of this nifty little symbol in the coming months. Although incorrect, we title this page and may sometimes refer to the symbol as True Position since this is typically the term people are referencing when they are looking for the specified tolerance. Depending on how it is called out, true position can mean several different things. It may apply to any feature of size Feature with physical dimensions like a hole, slot, boss or tab and control the central elements of these size features. In these examples, we will use holes, since these are the most common types of features controlled by true position. Position can be used on any feature of size but not on surfaces where we would use Profile. True Position â€"Location of a Feature Position in terms of the axis, point or plane defines how much variation a feature can have from a specified exact true location. The tolerance is a 2 or 3-Dimensional tolerance zone that surrounds the true location where a feature must lie. This means that you will have an exact point where the position should be and your tolerance specifies how far from this you can be. The true position is usually called out as a diameter to represent a circular or cylindrical tolerance zone. True position with a features of size can control the location, orientation and the size of the feature all at once. While true position on its own controls where the reference point locations need to lie, true position in MMC for a hole sets a minimum size and positional location of the hole to maintain functional control. It does this by allowing a bonus tolerance to be added to the part. As a part gets closer to the MMC, the constraints become tighter and the hole must be closer to its position. But, if the hole is a bit larger but still in spec , it can stray from its true position further and still allow proper function like a bolt passing though. True Position â€"Location of a feature A 2 dimensional cylindrical zone or, more commonly a 3-Dimensional cylinder, centered at the true position location referenced by the datums. The cylindrical tolerance zone would extend though the thickness of the part if this is a hole. A 3-Dimensional cylinder, centered at the true position location referenced by the datum surfaces. The cylindrical tolerance zone would extend though the thickness of the part if this is a through hole for the 3-dimensional tolerance zone similar to the RFS version. While this is the tolerance zone, the call-out now references the virtual condition of the entire part. True Position â€"Location of a Feature True position of a feature is made by first determining the current referenced point and then comparing that to any datum surfaces to determine how far off this true center the feature is. It is simplified like a dimensional tolerance but can be applied to a diameter tolerance zone instead of simple X-Y coordinates. This is done on a CMM or other measurement devices. The following formulas are used to create a gauge for true position under MMC. All gauge features should be located in the datum true positions, but sized according to the formulas above. Note on Bonus Tolerance: When a functional gauge is used for True Position, any difference the actual feature size is from the maximum material condition would be a bonus tolerance. The bonus tolerance for position then increases as the part gets closer to LMC. For instance, if you had a large hole size but was still in tolerance closer to LMC , you make more bonus tolerance for yourself making the true position tolerance larger. You can now have the hole center more out of position due to the bonus tolerance. For more detail on how bonus tolerances play into these callouts, see our sections on Maximum Material Condition. True Position â€"Location of a feature True position is closely related to symmetry and concentricity as they both require the location of features to be controlled. However, True position is more versatile since it can be called on a feature of size or combined with other geometric tolerances to specify an entire part envelope. The tolerance of both perpendicularity and true position now refers to the uniformity and cylindrical envelope of a central axis. See example 2 for more details. True Position â€"Location of a feature In example 1 you can see

how a hole can be called out using true position. However this can also be applied to anything in need of a location tolerance, such as a pin, a boss or even an edge of a part. When you have a hole in a part such as a bolted surface, true position is usually called out. It can be used almost anywhere to represent any feature of size. True position is also useful for describing and controlling a bolt pattern for a pipe fitting or a bolted fixture. If you specify the control using MMC, it allows you to have a pin gauge that you can insert into the part to see if the bolt pattern is functionally accurate. You will see true position called with MMC very commonly in bolt patterns where relative location of all the bolts and necessary clearance is critical. LMC with true position is a little less common, but often used when minimum wall thickness is desired. True Position â€"Location of Hole Example 1: Four holes are to be located on a block to ensure contact is always maintained and located within a specific position. The holes need to line up with the threaded connections in the mating part. The True position callout on a block With true position called out the holes do not need to be in exact positions as shown below, but their centers can vary by the amount specified by the tolerance. The basic dimensions dimensions in the squares are un-toleranced and describe the true location the hole would be in if it was perfect. In a 2D check of the upper right hole, the true location would be 40 mm from datum A and 40 mm from datum B. The holes center is calculated, usually by a CMM and compared to the true location. As long as the holes center is in the blue tolerance zone of 0. This means the entire hole must have its axis align with the datum. The tolerance zone would actually ensure that the location and the perpendicularity is within the specified tolerance. Since all the central points at any cross section are controlled by true position, the parts axis line between all central points would be controlled for orientation. The biggest thing to note about this design is that no matter what size hole you have, your true position would always have to be the same. This is ideal for when proper exact alignment is required for function of the part. It does, however, remove the possibility of using a functional gauge. Taking the same example, the true position can also be specified with a maximum material condition callout. This means you are now controlling the envelope of the entire hole feature, including the size of the hole throughout its entire depth. With an MMC callout you now can use a functional gauge to measure this part, to determine that the size and geometric tolerancing are within spec at the same time. Formula for a the functional gauge to measure the true position of all holes: Same specifications This would be the go gauge that would measure for hole size, orientation and position. The part would be pressed down onto the gauge and if it fits the part is in specification. Notice that datum A, B and C are all included in the gauge to check the location of the hole. Top view of the part once inserted into pin gauge As long as the gauge can go into the part, it is in spec. This makes it very easy to accurately gauge the part right on a production line. The function of the part is confirmed because as long as the surface that the part is bolted to has the same tolerances, it will always fit. Bonus Round Remember the further you are from MMC when it is referenced in the feature control frame, the more bonus tolerance you are allowed. Keep in mind the opposite is true for a positive feature like a pin, where the smaller the pin means you have more bonus tolerance. When true position is called out as a distance, you are permitted to move from the tolerance in X or Y direction by the allowed tolerance. However when done this way, the tolerance zone actually forms a square. This is usually undesirable since in the corners of the square are further from the center than the sides. Another common way true position can be called out is with slotted features. If you have a slot in your part that must always be located correctly, you can use true position to ensure that each of the planes that make up the slot are always located in the correct position. Symmetry can also be used in this case â€" but only if the slots have a referenced datum plane that they are symmetrical about and measuring symmetry is very difficult!

DOWNLOAD PDF 27 VIRTUAL GAGE WITH INTERNAL MOBILITIES FOR THE VERIFICATION OF FUNCTIONAL SPECIFICATIONS

Chapter 7 : True Position | GD&T Basics

In this paper, we propose a model making it possible to build a virtual gauge with internal mobilities, and to specify a part, a mechanism or a manufacturing process.

System testing Documentation Integration with other building systems such as lighting, fire and life safety, security, and factory-installed equipment controls Integration with other enterprise level applications, such as facility management, preventive maintenance, or energy management systems. The guideline does not include specifying control of fire or life safety systems or equipment, nor does it include specifying security systems or enterprise level applications. SGPC 13 to maintain and revise Guideline Guideline on continuous maintenance. Measurement of Energy, Demand and Water Savings 1. The purpose of this document is to provide guidelines for reliably measuring the energy, demand and water savings achieved in conservation projects. This guideline provides the basis for selecting and sizing control dampers outdoor, return, and relief commonly found in constant volume CAV and variable air volume VAV air-handling units and systems with air-side economizers. The purpose of this document is to provide heating, ventilation, and air conditioning HVAC and battery system designers and users with information and recommendations concerning the ventilation and thermal management of stationary battery installations. The scope of this document includes only stationary batteries under conditions of expected use. Multiple operating modes are identified. The ventilation practices described in this guide represent the "best practice" based on the information available at the time this document was developed. These recommendations were developed without consideration of economics, availability of equipment and personnel, or relative importance of the application. Design of a ventilation system for a specific battery installation requires consideration of all issues, not just the technical issues considered in this document. This guideline defines recommended methods for measuring chilled-water plant thermal load and energy use and for calculating chilled water plant efficiency. They do not discuss the comparison of collected data between different sites, nor do they recommend that data obtained be applied in this manner. To establish minimum recommended design guidelines necessary to achieve an acceptable level of performance and safety for heating, ventilation and air conditioning equipment used on rail passenger vehicles operating in the unique and demanding environment of rail transportation systems. This Guideline covers rail passenger vehicles used in regularly scheduled public transportation service. The Guideline will address environmental conditions, equipment configurations, air filtration, temperature and humidity controls, determination and verification of heating and cooling capacity, ventilation standards, passenger comfort criteria, materials, packaging, noise, vibration and shock, refrigerant selection,, energy efficiency, corrosion protection, voltage and electrical requirements, power supply and electromagnetic interference. SCOPE This guideline primarily applies to ventilation and IAQ for human occupancy in residential buildings three stories or fewer in height above grade, including manufactured and modular houses. This guideline provides recommended procedures for effective measurement of airborne gas and vapor concentrations inside commercial buildings. Its goal is to provide consistent procedures to follow so field measurements of contaminant concentrations are accurate and reproducible, avoiding typical problems that may cause unreliable or inconsistent results. This document provides guidance on the procedures to follow when measuring gas-phase concentrations of contaminants in commercial buildings. The subject measurements are those used to establish existing, baseline or changed conditions as a function of the building systems or interior environments. The methods in this guideline emphasize obtaining meaningful data within a reasonable time period at a reasonable cost. This guideline does not apply to industrial or residential buildings. It does not address: Air Quality Within Commercial Aircraft 1. This Guideline serves as a companion to ASHRAE Standard and provides supplemental information on air quality in air-carrier aircraft and on measurement and testing related to aircraft air quality. Guideline 28 placed on continuous maintenance January To provide guidance for the practical evaluation, design, and implementation of measures to reduce multiple risks in new

and existing buildings. Specific subject areas of concern include air, food, and water. The extraordinary events addressed in this guideline include fire, seismic events, chemical and biological releases, blast, and other extraordinary hazards. The guideline will address extraordinary incidents from a multi-hazard perspective, and will cover both intentional and accidental occurrences. The guideline addresses aspects of building performance that affect occupant health and safety, including egress; chemical, biological, and radiological CBR protection; fire protection; smoke removal or purging; filtration; air quality; entrance paths for contaminants; and building envelopes. Scope This guideline applies to the ongoing operational practices for building assemblies and systems, particularly with respect to energy efficiency, water consumption, productivity, occupant comfort, indoor air quality IAQ , health and safety. Guideline RA - Published Guideline. This guideline establishes a method and format for documenting inputs, assumptions, methods and outputs utilized when conducting indoor airflow and contaminant transport modeling studies. This guideline applies to the application of airflow and contaminant modeling for analyses of indoor air quality, thermal comfort, energy and events related to chemical, biological and radiological agents. This guideline only applies to modeling efforts using multizone network models, computational fluid dynamics CFD or combinations of the two. TPS change approved February 28, The purpose of this guideline is to establish a consistent methodology to determine the energy consumption created by the introduction of air cleaning and filtration devices into an air stream. The purpose of this guideline is to provide uniform sequences of operation for heating, ventilating, and air-conditioning HVAC systems that are intended to maximize HVAC system energy efficiency and performance, provide control stability, and allow for real-time fault detection and diagnostics. The purpose of this guideline is to provide information and recommendations for dosing, placement and safe usage of Upper-Air UV-C devices. This Guideline is intended to establish a test procedure utilizing metal pressure vessels for the evaluation of materials used in refrigeration systems. This Guideline describes the preparation of metal pressure vessels, and the procedure for charging them with refrigerant and with the materials to be tested. A procedure for heating the metal vessel and regulating the pressure is described. The technique described can be used for evaluating many different types of materials. The guideline does not describe the detailed preparation of the materials to be tested prior to placing them in the metal vessel. The materials to be tested can be aged over a broad range of temperatures and pressures, which fall within the safety limits of the vessel. Detailed safety precautions are included. Properly performing this test requires careful attention to the detailed experimental technique, and careful adherence to safety procedures. The purpose of this guideline is to recommend uniform test methods and procedures for experimentally determining the fractionated vapor and liquid compositions of refrigerant blends under simulated leakage from containers and equipment in storage, transport, operation and service. The WCFF with respect to toxicity is used to determine the toxicity safety class of refrigerant blends whose component refrigerants are not assigned the same toxicity safety group class. This guideline defines a standardized test apparatus, method, and procedures for experimentally conducting fractionation analyses of refrigerant blends that is consistent with their thermodynamic vapor-liquid equilibrium VLE properties: Guideline - Published Guideline. Refrigeration Oil Description Purpose: The purpose of this guideline is to describe lubricants used in refrigeration and air-conditioning systems based on molecular structure, physical properties, and chemical properties. This guideline defines those properties critical to the precise identification of refrigeration lubricants, along with recognized test procedures for the determination of these properties. This guideline applies to lubricants used or proposed as compressor lubricants in refrigerating systems. This guideline provides recognized test methods intended to: This guideline is not intended to define refrigeration oil quality through the establishment of test specifications or requirements. In addition, performance tests intended to measure quality have been excluded from this guideline. This guideline provides guidance for the design, installation and commissioning of Variable Refrigerant Flow VRF systems. Editorial change to the title approved July 31, The purpose of this guideline is to recommend measures that exceed minimum requirements for improving indoor air quality in commercial and institutional buildings. These measures are intended to provide enhanced

indoor air quality that is acceptable to human occupants and that minimizes adverse health effects. This standard specifies safe design, construction, installation, and operation of refrigeration systems. SSPC 15 to maintain and revise Standard Standard on continuous maintenance. Safety Standard for Refrigeration Systems Purpose: This standard specifies safe design, construction, installation and operation of refrigeration systems. Authorized January 28, This standard specifies safe design, installation, operation and maintenance of air-conditioning systems in residential applications. This standard establishes safeguards for life, limb, health and property and prescribes safety requirements. This standard applies to the design, installation, operation and maintenance of mechanical air-conditioning and heat pump systems installed in stationary applications that include: PURPOSE The purpose of this standard is to prescribe test methods for determining the cooling and heating capacity of room air conditioners, packaged terminal air conditioners and packaged terminal heat pumps. SCOPE establishes uniform methods of testing to obtain rating data, specifies test equipment for performing such tests, specifies data required and calculations to be used, and lists and defines the terms used in testing. This standard prescribes a method of testing the capacity of thermostatic refrigerant expansion valves for use in vapor-compression refrigeration systems. The purposes of this standard are: This standard prescribes methods of laboratory testing to measure the heat rejection capabilities of remote mechanical-draft, air-cooled refrigerant condensers for refrigerating and air conditioning. The objective is to ensure uniform performance information for establishing ratings. This standard prescribes methods of laboratory testing remote mechanical-draft, air-cooled refrigerant condensers. This standard prescribes methods of testing the thermal performance and liquid-side pressure drop of liquid cooled refrigerant condensers. This standard applies to the methods of testing for thermodynamic performance rating of liquid-cooled refrigerant condensers that operate at subcritical pressures of the refrigerant. PURPOSE The purpose of this standard is to provide methods of testing for rating the thermodynamic performance of positive displacement refrigerant compressors and condensing units that operate at subcritical temperatures of the refrigerant.

Chapter 8 : TPS - Titles, Purposes, and Scopes

Note: OCR errors may be found in this Reference List extracted from the full text article. ACM has opted to expose the complete List rather than only correct and linked references.

Chapter 9 : A High Performance Multifunction Calibrator

True position of a feature of size under MMC is used when a functional gauge is ideal for checking the part. True position is also useful for describing and controlling a bolt pattern for a pipe fitting or a bolted fixture.