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Chapter 1 : /, , and Assembly Language Programming - Ebook pdf and epub

*Assembly Language Programming for the Intel 80Xxx Family (Macmillan Programming Languages Series) [William B. Giles] on calendrierdelascience.com *FREE* shipping on qualifying offers.*

The processor seems ideal for this purpose. There is a lot of programming info and development tools for the and huge amounts of sample code. The plan is to build a simple reference design that is relatively modular and can be expanded from a library of additional functional blocks, i. The SBC will have a simplified architecture: Features like Timers, DMA, and complex Interrupt architectures can be added as needed, but should be bolt-on modular components. Back when the XT line of motherboards were going obsolete, I salvaged a lot of processors and the support chips for them. These parts used to be virtually free, because the , the , the , etc. April 20, The schematics have been updated to final wiring versions. The design has been split onto two boards no longer qualified as a single board design?? The CPU board has been wired. Update The project has remained dormant for an extended period. This would be a big improvement over the design presently described on this page, because clock chips are far more scarce than the processor itself. Further, I have found an embedded tools developer who has kindly made available a simple Intel assembler that makes it easy to map ROM firmware directly to hard-coded addresses. He also has offered to make available a monitor binary that could run on the Single Board Computer. I need to graft on a serial port to the design to act as console. News I have put together an update page that you can go to, to see any news I have regarding the project. Antonakos came out with a decent design for an SBC which has been incorporated into his textbook. This book is invaluable as a resource, and incorporates a detailed study of his SBC design. It also has most of the IC datasheets reprinted in it that are needed to complete a hardware design. Some of us code closer to the bare metal than that. The FAQ for the comp. Jack Klein provides some helpful links on his Intel x86 Page. This book is a good user-friendly introduction, although he tends to stay mired at a very introductory level throughout the entire book. Also, I found myself disappointed by his limited coverage of how to get actual practical software up and running on his design. The Antonakos book is the reference I am using the most now. For general coverage of assembly language programming of the 80x86 family, the book I like the most is William B. All three of these books are older, and used copies can usually be found at a low cost. I may be contacted at This Address.

Chapter 2 : Scott's Single Board Computer Project Page

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For example, AMD architecture uses only the lower 48 bits of an address, and bits 48 through 63 must be a copy of bit 47 or the processor raises an exception. Another downside is that addressing all 64 bits of memory requires a lot more paging tables for the OS to store, using valuable memory for systems with less than all 16 exabytes installed. Note these are virtual addresses, not physical addresses. As a result, many operating systems use the higher half of this space for the OS, starting at the top and growing down, while user programs use the lower half, starting at the bottom and growing upwards. The resulting addressing is shown in Figure 2. The resulting addresses are not too important for user programs since addresses are assigned by the OS, but the distinction between user addresses and kernel addresses are useful for debugging. A final OS-related item relates to multithreaded programming, but this topic is too large to cover here. The only mention is that there are memory barrier opcodes for helping to keep shared resources uncorrupted. Figure 2 - Memory Addressing Calling Conventions Interfacing with operating system libraries requires knowing how to pass parameters and manage the stack. These details on a platform are called a calling convention. XMM0, 1, 2, and 3 are used for floating point arguments. Additional arguments are pushed on the stack left to right. Parameters less than 64 bits long are not zero extended; the high bits contain garbage. Integer return values similar to x86 are returned in RAX if 64 bits or less. Floating point return values are returned in XMM0. Larger return values structs have space allocated on the stack by the caller, and RCX then contains a pointer to the return space when the callee is called. Register usage for integer parameters is then pushed one to the right. RAX returns this address to the caller. The stack is byte aligned. Note there is no calling convention for the floating point and thus MMX registers. Examples Armed with the above, here are a few examples showing x64 usage. The first is a simple x64 standalone assembly program that pops up a Windows MessageBox. Start which makes a windows executable and links with appropriate libraries. Run the resulting executable hello. Other compiler systems are similar. First make sure your compiler is an xcapable version. Under Active Platform, select New Under Platform, select x If it does not appear figure out how to add the bit SDK tools and repeat. Compile and step into the code. Create an assembly file, and add it to the project. It defaults to a 32 bit assembler which is fine. Open the assembly file properties, select all configurations, and edit the custom build step. Put command line ml For example, in main. We duplicate that functionality in assembly in a separate file CombineA. Conclusion This has been a necessarily brief introduction to x64 assembly programming. Volume 1 contains the architecture details and is a good start if you know assembly. Other places are assembly books or online assembly tutorials. To get an understanding of how your code executes, it is instructive to step through code in debugger, looking at the disassembly, until you can read assembly code as well as your favorite language. Finally, read the forums at masm

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Chapter 3 : Record of Courses Taken in Preparation for Ph

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Switching modes[edit] The processor runs in real mode immediately after power on, so an operating system kernel , or other program, must explicitly switch to another mode if it wishes to run in anything but real mode. In general, the features of the modern x86 instruction set are: A compact encoding Variable length and alignment independent encoded as little endian , as is all data in the x86 architecture Mainly one-address and two-address instructions, that is to say, the first operand is also the destination. Both general and implicit register usage; although all seven counting ebp general registers in bit mode, and all fifteen counting rbp general registers in bit mode, can be freely used as accumulators or for addressing, most of them are also implicitly used by certain more or less special instructions; affected registers must therefore be temporarily preserved normally stacked , if active during such instruction sequences. Produces conditional flags implicitly through most integer ALU instructions. Supports various addressing modes including immediate, offset, and scaled index but not PC-relative, except jumps introduced as an improvement in the x architecture. Includes floating point to a stack of registers. Stack instructions[edit] The x86 architecture has hardware support for an execution stack mechanism. Instructions such as push, pop, call and ret are used with the properly set up stack to pass parameters, to allocate space for local data, and to save and restore call-return points. The ret size instruction is very useful for implementing space efficient and fast calling conventions where the callee is responsible for reclaiming stack space occupied by parameters. Whether it is faster or slower depends on the particular xprocessor implementation as well as the calling convention used by the compiler, programmer or particular program code; most x86 code is intended to run on xprocessors from several manufacturers and on different technological generations of processors, which implies highly varying microarchitectures and microcode solutions as well as varying gate - and transistor -level design choices. Floating-point instructions[edit] x86 assembly language includes instructions for a stack-based floating-point unit FPU. The FPU was an optional separate coprocessor for the through the , it was an on-chip option for the series, and it is a standard feature in every Intel x86 CPU since the , starting with the Pentium. The FPU instructions include addition, subtraction, negation, multiplication, division, remainder, square roots, integer truncation, fraction truncation, and scale by power of two. The operations also include conversion instructions, which can load or store a value from memory in any of the following formats: The stack register to stack register format of the instructions is usually fop st, st n or fop st n , st, where st is equivalent to st 0 , and st n is one of the 8 stack registers st 0 , st 1 , Like the integers, the first operand is both the first source operand and the destination operand. The addition, subtraction, multiplication, division, store and comparison instructions include instruction modes that pop the top of the stack after their operation is complete. Various instruction technologies support different operations on different register sets, but taken as complete whole from MMX to SSE4. So for example, paddw mm0, mm1 performs 4 parallel bit indicated by the w integer adds indicated by the padd of mm0 values to mm1 and stores the result in mm0. Some other unusual instructions have been added including a sum of absolute differences used for motion estimation in video compression , such as is done in MPEG and a bit multiply accumulation instruction useful for software-based alpha-blending and digital filtering. These instruction sets also include numerous fixed sub-word instructions for shuffling, inserting and extracting the values around within the registers. Data manipulation instructions[edit] The x86 processor also includes complex addressing modes for addressing memory with an immediate offset, a register, a register with an offset, a scaled register with or without an offset, and a register with an optional offset and another scaled register. In general x86 processors can load and use memory matched to the size of any register it is operating on. The SIMD instructions also include half-load instructions. The implicit segment registers used are ds for si and es for di. The cx or ecx register is used as a decrementing counter, and the

operation stops when the counter reaches zero or for scans and comparisons when inequality is detected. The stack is implemented with an implicitly decrementing push and incrementing pop stack pointer. In bit mode, this implicit stack pointer is addressed as SS: The stack pointer actually points to the last value that was stored, under the assumption that its size will match the operating mode of the processor i. This code in the beginning of a function: Values for a SIMD load or store are assumed to be packed in adjacent positions for the SIMD register and will align them in sequential little-endian order. Some SSE load and store instructions require byte alignment to function properly. The SIMD instruction sets also include "prefetch" instructions which perform the load but do not target any register, used for cache loading. The SSE instruction sets also include non-temporal store instructions which will perform stores straight to memory without performing a cache allocate if the destination is not already cached otherwise it will behave like a regular store. Most generic integer and floating point but no SIMD instructions can use one parameter as a complex address as the second source parameter. Integer instructions can also accept one memory parameter as a destination operand. Program flow[edit] The x86 assembly has an unconditional jump operation, jmp , which can take an immediate address, a register or an indirect address as a parameter note that most RISC processors only support a link register or short immediate displacement for jumping. Many arithmetic and logic operations set, clear or complement these flags depending on their result. The comparison cmp compare and test instructions set the flags as if they had performed a subtraction or a bitwise AND operation, respectively, without altering the values of the operands. There are also instructions such as clc clear carry flag and cmc complement carry flag which work on the flags directly. Floating point comparisons are performed via fcom or ficom instructions which eventually have to be converted to integer flags. Each jump operation has three different forms, depending on the size of the operand. A short jump uses an 8-bit signed operand, which is a relative offset from the current instruction. A near jump is similar to a short jump but uses a bit signed operand in real or protected mode or a bit signed operand in bit protected mode only. A far jump is one that uses the full segment base: There are also indirect and indexed forms of each of these. In addition to the simple jump operations, there are the call call a subroutine and ret return from subroutine instructions. Before transferring control to the subroutine, call pushes the segment offset address of the instruction following the call onto the stack; ret pops this value off the stack, and jumps to it, effectively returning the flow of control to that part of the program. In the case of a far call, the segment base is pushed following the offset; far ret pops the offset and then the segment base to return. There are also two similar instructions, int interrupt , which saves the current E FLAGS register value on the stack, then performs a far call, except that instead of an address, it uses an interrupt vector, an index into a table of interrupt handler addresses. Typically, the interrupt handler saves all other CPU registers it uses, unless they are used to return the result of an operation to the calling program in software called interrupts. The matching return from interrupt instruction is iret, which restores the flags after returning. Soft Interrupts of the type described above are used by some operating systems for system calls, and can also be used in debugging hard interrupt handlers. Hard interrupts are triggered by external hardware events, and must preserve all register values as the state of the currently executing program is unknown. In Protected Mode, interrupts may be set up by the OS to trigger a task switch, which will automatically save all registers of the active task. Examples[edit] This article possibly contains original research. Please improve it by verifying the claims made and adding inline citations. Statements consisting only of original research should be removed. March "Hello world! This will be argument to printf call printf ;calls printf add esp, 4 ;advances stack-pointer by 4 flushing out the pushed string argument ret ;return "Hello world! When a comparison is made between two data, the CPU sets the relevant flag or flags. Following this, conditional jump instructions can be used to check the flags and branch to code that should run, e. For example, to disable all maskable interrupts, you can use the instruction: The low 8 bits of the flag register can be loaded into ah using the lahf instruction. The entire flags register can also be moved on and off the stack using the instructions pushf, popf, int including into and iret. Using the instruction pointer register[edit] The instruction pointer is called ip in bit mode, eip in bit mode, and rip in bit mode.

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Chapter 4 : x86 assembly language - Wikipedia

x86 assembly language is a family of backward-compatible assembly languages, which provide some level of compatibility all the way back to the Intel introduced in April x86 assembly languages are used to.

C Flags The Intel is the successor to the It uses the same basic instruction set and register model as the developed by Computer Terminal Corporation , even though it is not source-code compatible nor binary-compatible with its predecessor. Every instruction in the has an equivalent instruction in the even though the actual opcodes differ between the two CPUs. The also adds a few bit operations in its instruction set as well. Whereas the required the use of the HL register pair to indirectly access its bit memory space, the added addressing modes to allow direct access to its full bit memory space. In addition, the internal 7-level push-down call stack of the was replaced by a dedicated bit stack-pointer SP register. Registers[edit] The processor has seven 8-bit registers A, B, C, D, E, H, and L , where A is the primary 8-bit accumulator, and the other six registers can be used as either individual 8-bit registers or as three bit register pairs BC, DE, and HL, referred to as B, D and H in Intel documents depending on the particular instruction. Some instructions also enable the HL register pair to be used as a limited bit accumulator, and a pseudo-register M can be used almost anywhere that any other register can be used, referring to the memory address pointed to by the HL pair. Flags[edit] The processor maintains internal flag bits a status register , which indicate the results of arithmetic and logical instructions. Sign S , set if the result is negative. Zero Z , set if the result is zero. Parity P , set if the number of 1 bits in the result is even. Carry C , set if the last addition operation resulted in a carry or if the last subtraction operation required a borrow Auxiliary carry AC or H , used for binary-coded decimal arithmetic BCD. The carry bit can be set or complemented by specific instructions. Conditional-branch instructions test the various flag status bits. The flags can be copied as a group to the accumulator. The A accumulator and the flags together are called the PSW register, or program status word. Some of them are followed by one or two bytes of data, which can be an immediate operand, a memory address, or a port number. Like larger processors, it has automatic CALL and RET instructions for multi-level procedure calls and returns which can even be conditionally executed, like jumps and instructions to save and restore any bit register pair on the machine stack. There are also eight one-byte call instructions RST for subroutines located at the fixed addresses 00h, 08h, 10h, These were intended to be supplied by external hardware in order to invoke a corresponding interrupt service routine , but were also often employed as fast system calls. The most sophisticated command is XTHL, which is used for exchanging the register pair HL with the value stored at the address indicated by the stack pointer. For 8-bit operations with two operands, the other operand can be either an immediate value, another 8-bit register, or a memory byte addressed by the bit register pair HL. Direct copying is supported between any two 8-bit registers and between any 8-bit register and an HL-addressed memory byte. Due to the regular encoding of the MOV instruction using a quarter of available opcode space , there are redundant codes to copy a register into itself MOV B,B, for instance , which were of little use, except for delays. However, what would have been a copy from the HL-addressed cell into itself i. By adding HL to itself, it is possible to achieve the same result as a bit arithmetical left shift with one instruction. IN 05h would put the address h on the bit address bus. Separate stack space[edit] One of the bits in the processor state word see below indicates that the processor is accessing data from the stack. Using this signal, it is possible to implement a separate stack memory space. However, this feature was seldom used. The internal state word[edit] For more advanced systems, during one phase of its working loop, the processor set its "internal state byte" on the data bus. The interrupt system state enabled or disabled is also output on a separate pin. For simple systems, where the interrupts are not used, it is possible to find cases where this pin is used as an additional single-bit output port the popular RadioRK computer made in the Soviet Union , for instance. The data block is copied one byte at a time, and the data movement and looping logic utilizes bit operations. Using the two additional pins read and write signals , it is possible to assemble simple

microprocessor devices very easily. Only the separate IO space, interrupts and DMA require additional chips to decode the processor pin signals. However, the processor load capacity is limited, and even simple computers frequently contained bus amplifiers. The processor consumes about 1.

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Chapter 5 : dword - Wiktionary

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Chapter 6 : Introduction to x64 Assembly | IntelÂ® Software

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Chapter 7 : CS Computer Organization and Assembly Language Programming (4)

** , William B. Giles, Assembly language programming for the Intel 80XXX family On line 7, "X" and "Y" are defined to be qwords. Therefore, each is eight bytes long â€" the size of a double in C.*

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THE INTEL MICROPROCESSORS striving to function in a field of study that uses computers must understand assembly language programming, a version of C language, and.