DOWNLOAD PDF RAPID THERMAL AND OTHER SHORT TIME PROCESSING

Chapter 1 : Unit Operations in Food Processing - R. L. Earle

Get this from a library! Rapid thermal and other short-time processing technologies: proceedings of the international symposium. [Fred Roozeboom; Electrochemical Society.

A single furnace accepts many wafers at the same time, in a specially designed quartz rack called a "boat". Historically, the boat entered the oxidation chamber from the side this design is called "horizontal" , and held the wafers vertically, beside each other. However, many modern designs hold the wafers horizontally, above and below each other, and load them into the oxidation chamber from below. Vertical furnaces stand higher than horizontal furnaces, so they may not fit into some microfabrication facilities. However, they help to prevent dust contamination. Unlike horizontal furnaces, in which falling dust can contaminate any wafer, vertical furnaces use enclosed cabinets with air filtration systems to prevent dust from reaching the wafers. Vertical furnaces also eliminate an issue that plagued horizontal furnaces: Horizontal furnaces typically have convection currents inside the tube which causes the bottom of the tube to be slightly colder than the top of the tube. As the wafers lie vertically in the tube the convection and the temperature gradient with it causes the top of the wafer to have a thicker oxide than the bottom of the wafer. Vertical furnaces solve this problem by having wafer sitting horizontally, and then having the gas flow in the furnace flowing from top to bottom, significantly damping any thermal convections. Vertical furnaces also allow the use of load locks to purge the wafers with nitrogen before oxidation to limit the growth of native oxide on the Si surface. Oxide quality[edit] Wet oxidation is preferred to dry oxidation for growing thick oxides, because of the higher growth rate. However, fast oxidation leaves more dangling bonds at the silicon interface, which produce quantum states for electrons and allow current to leak along the interface. This is called a "dirty" interface. Wet oxidation also yields a lower- density oxide, with lower dielectric strength. The long time required to grow a thick oxide in dry oxidation makes this process impractical. Thick oxides are usually grown with a long wet oxidation bracketed by short dry ones a dry-wet-dry cycle. The beginning and ending dry oxidations produce films of high-quality oxide at the outer and inner surfaces of the oxide layer, respectively. However, chlorine can immobilize sodium by forming sodium chloride. Chlorine is often introduced by adding hydrogen chloride or trichloroethylene to the oxidizing medium. Its presence also increases the rate of oxidation. Other notes[edit] Thermal oxidation can be performed on selected areas of a wafer, and blocked on others. Areas which are not to be oxidized are covered with a film of silicon nitride , which blocks diffusion of oxygen and water vapor due to its oxidation at a much slower rate. This process cannot produce sharp features, because lateral parallel to the surface diffusion of oxidant molecules under the nitride mask causes the oxide to protrude into the masked area. Because impurities dissolve differently in silicon and oxide, a growing oxide will selectively take up or reject dopants. This redistribution is governed by the segregation coefficient , which determines how strongly the oxide absorbs or rejects the dopant, and the diffusivity [SIA disambiguation needed]. The orientation of the silicon crystal affects oxidation. For instance, in MOSFET processes, thermal oxidation is never performed after the doping for the source and drain terminals is performed, because it would disturb the placement of the dopants.

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Chapter 2 : Millisecond Anneal - Mattson Technology, Inc.

Rapid Thermal and Other Short Time Processing: Proceedings of the International Symposium (Electrochemical Society Proceedings) [Ont.) International Symposium on Rapid Thermal and Other Short-Time Processing Technologies (1st: Toronto, Fred Roozeboom, Electrochemical Society Electronics Division, Electrochemical Society.

A substrate, such as a semiconductor wafer, coated with a layer of coating material is heated to an elevated temperature at a heating rate of greater than about 20 DEG C per second. Once the coating material has been converted to a low dielectric constant material with desired properties, the coated substrate is cooled. Alternatively, spike heating raises and promptly lowers the temperature of the coated substrate to effect curing in one or a series of spikes heating steps. The method allows for a thinner refractory barrier metal layer thickness to prevent copper diffusion, and uses shorter curing times resulting in higher throughput. Field of the Invention This invention relates to the formation of low dielectric constant "low k" layers suitable for use in semiconductor devices, and more particularly, to a method for curing low k dielectric materials using very short, relatively high temperature cycles. Background of the Invention Semiconductor chips are used in many applications, including as processor chips for computers, as integrated circuits, and as flash memory for hand held computing devices, wireless telephones, and digital cameras. Regardless of the application, ideally a semiconductor chip holds as many circuits or memory cells as possible per unit area. In this way, the size, weight, and energy consumption of devices that use semiconductor chips are minimized, while nevertheless improving the memory capacity and computing power of the devices. The escalating requirements for high density and performance associated with ultra-large scale integration semiconductor devices necessitate design features of 0. A common circuit component of semiconductor chips is the transistor. In ultra-large-scale integrated ULSI semiconductor chips, a transistor is established by forming a polysilicon gate on a silicon substrate, and then forming a source region and a drain region side by side in the substrate beneath the gate by implanting appropriate dopant materials into the areas of the substrate that are to become the source and drain regions. The gate is insulated from the source and drain regions by a thin gate oxide layer. This generally-described structure cooperates to function as a transistor. A conventional method for forming patterned metal layers comprises a subtractive etching or etch back step as the primary metal forming technique. A metal layer is deposited on the first dielectric layer and patterned using photolithographic masking and etching techniques to form a desired conductive pattern comprising a metal feature separated by gaps, such as a plurality of metal lines with inter-wiring spacings therebetween. A dielectric layer is then applied to the resulting conductive pattern to fill in the gaps. The surface thereof is then planarized by conventional etching or chemical-mechanical polishing CMP techniques. A through-hole is then formed in the dielectric layer to expose a selected portion of an underlying metal feature. The exposed portion of the metal feature at the bottom of the through-hole serves as a contact pad. Upon filling the through-hole with conductive material, such as a metal plug, to form a conductive via, the bottom surface of the conductive via is in electrical contact with the underlying metal feature. Many ultra large scale integration ULSI devices presently manufactured are very complex and require multiple levels of metallization for interconnections. It has been common to repeat the above-described via formation process multiple times, e. As semiconductor devices become smaller, and on-chip device density correspondingly increases, signal delays due to capacitive coupling and crosstalk between closely spaced metal lines are increasing. These problems are exacerbated by the need to keep conductor lines as short as possible in order to minimize transmission delays, thus requiring multi-level wiring schemes for the chip. As a consequence, capacitive coupling between conductive lines significantly limits circuit speed. A problem encountered in highly miniaturized semiconductor devices employing multiple metallization levels and reduced inter-wiring spacings in both the horizontal and vertical dimensions is related to the resistance-capacitance RC time constant of the system. If intra-metal capacitance is high, electrical inefficiencies and inaccuracies increase. It has been recognized that a reduction in capacitance within the

multi-level metallization system will reduce the RC time constant between the conductive lines. The dielectric constant is based on a scale where 1. As used herein, the term "low k" will refer to materials that have dielectric constants less than 3. The drive to reduce the RC delay associated with the metal interconnect lines also has led the industry to move away from the traditional aluminum Al interconnect metal lines in favor of copper Cu based metallization. The sheet resistivity of copper-based metal lines can be half that of aluminum-based metal systems. However, copper diffuses more easily into the inter-level dielectric at normal processing temperatures, thereby degrading the dielectric and weakening the isolation between adjacent metal lines. If the copper diffuses into the underlying silicon, then the device performance also will be degraded. To prevent unwanted diffusion, most copper processes e. For very narrow copper lines, applying an appropriate refractory barrier metal layer is very important. Thick barrier layers can result in higher metal line resistance than found in Al lines. Therefore, the thickness of the barrier layer must be minimized. The drive towards increased miniaturization and the resultant increase in the RC time constant also have served as an impetus for the development of newer, low dielectric constant "low k" materials as substitutes for conventional higher dielectric constant silicon oxide-based ILD materials. The ILD films or layers must normally be formed at relatively low temperatures in order to avoid damage to or destruction of underlying conductors. Lower processing temperatures can increase the time needed for layer formation leading to decreased manufacturing throughput. One prior process for applying low k materials to semiconductor substrates is shown in U. First, a layer of low k material resin combined with a solvent or dispersant therefor is applied to a substrate by a spin coating process. The method shown in U. Temperature ramp up and ramp down of the coated substrate is controlled by regulating the spacing between the hot plates and the substrate, and controlling the length of time the substrate is held at a certain spacing. For baking, curing and cooling the coated substrate, three hot plates of different temperatures are used. The substrate is processed sequentially by being transferred between the hot plates. In view of this transporting, the heating of the substrate is not controlled as precisely and rapidly as is desirable for substrates that include copper interconnects. See EP 0 A2. Such typical furnace curing processes place severe demands on process integration. Long cure times result in decreased manufacturing throughput. However, increasing cure temperatures to reduce cure times can cause damage to, or even destroy, underlying conductors. In addition, it is difficult to suppress copper diffusion for a long duration cure, even when the cure is carried out at a lower temperature. Nevertheless, higher curing temperatures can also lead to increased copper diffusion rates. Other deficiencies of the current processes include inadequate control of the thermal budget. Although the curing is described as rapid, the curing times used are up to ten minutes, which is long enough to cause undesirable diffusion of metal interconnects sought to be avoided. The processing described would be particularly undesirable for copper interconnects. See also related U. Thus, there exists a need for a method of forming a layer of low dielectric constant material on a surface of a substrate characterized by shorter curing times, higher curing temperatures, and precise control of thermal budget without the requirement of a thicker refractory barrier metal layers. The coated substrate is held at the elevated temperature for a first time interval sufficient to convert the coating material to a low dielectric constant material of high thermal stability. The purpose of curing step b is mainly to initiate the chemical reaction s that produce films with high thermal stability. For most films, step b has very little or no effect on the dielectric constant, meaning that the k value remains nearly unaffected after the cure. Before curing, a pre-heating or baking step can be carried out to evaporate any solvents remaining in the coating material. Preferably, the baking step temperature is lower than the elevated temperature. The first time interval of curing step b is generally shorter than that used in prior art methods. Depending upon the low dielectric constant material low k material used, the temperature-time curve with which the substrate is processed, the gas atmosphere in which the substrate is processed, and the heating method, the first time interval is preferably less than 30 seconds, more preferably less than 25 seconds, and under certain conditions even less than 20 seconds. Preferably, the substrate is heated in a lamp-based RTP apparatus, wherein heating is by electromagnetic radiation, e. The electromagnetic radiation, or at least part of it, also can be generated by

laser. Due to the high heating rate of the curing step, the first time interval for holding the coated substrate at an elevated temperature advantageously can be reduced. When heating is by UV radiation, the first time interval can be reduced to as short as 20 seconds. The present invention also can be carried out using "susceptor-based RTP" systems that do not employ lamps to achieve rapid heating rates. One example of such a "susceptor-based RTP" system is described in U. The wafer is rapidly inserted into a furnace cavity maintained at a substantially constant processing temperature, controllably heated by electrical heating means, preferably resistor heating means. Due to the rapid insertion, the wafer rapidly heats to the desired process temperature. The first time interval of curing step b is sufficient to at least partially convert the coated material into a thermally stable low k material film. If the coated substrate is heated only once to the elevated temperature, without stepped intervals, the first time interval is selected such that within this time the material is fully converted. In spiking processes, the first time interval may be less than one second, depending upon the heating apparatus used. In spiking processes according to this invention, the first time interval of curing step b is determined by the change from heating to cooling, and can even be reduced to below one second, such as about 0. The present invention also embraces temperature-time processes in which the coated substrate is heated to various elevated temperatures in a sequence of time intervals. The time intervals can comprise intervals in which the substrate is cooled down to lower temperatures. Multiple spike processing, in which one spike is followed by at least one other spike, may be used. The time interval between two spike processes, meaning the time interval between subsequent rapid cooling and rapid heating, is preferably less than about 30 seconds, and can be as short as about 0. In multiple spike processes, it can be sufficient for the coating material to be only partially converted into low k material within one spike process or within one time interval in which the substrate is heated to an elevated temperature because the coated material will be fully converted in a following time interval or spike process in the sequence. An elevated temperature is selected within a temperature range embracing the lowest temperature at which curing of the coating material starts at the chosen process parameters and the highest temperature at which the coating material starts to decompose. Process parameters that may impact the chosen elevated temperature range include atmosphere content and pressure, coating material composition, heating rate, and spectrum of electromagnetic radiation selected for heating. Ideally, the highest temperature in the temperature range is lower than the decomposition temperature of the coating material to account for the possibility that the heating will not be uniform across the substrate. This will ensure that the low k material does not decompose even if the temperature distribution across the substrate is not uniform. Preferably, the curing time interval is 60 seconds or less, most preferably about 30 seconds. Preferably, the gas atmosphere in which the coated substrate is processed is dominated by an inert gas. Depending upon the temperature, molecular nitrogen can be used as the inert gas. However, noble gases argon and helium or noble gases mixed with nitrogen can be used. As one possibility, with the beginning of the temperature ramp down, the composition of the atmosphere can be changed by adding helium to the nitrogen gas. The thermal conductivity can be increased by adding helium, which helps to speed the cooling rate. If the coating or low k material does not react with molecular hydrogen gas, such gas also can be introduced to manipulate the thermal conductivity of the process atmosphere. In addition, added hydrogen gas or ammonia can prevent oxidation of the coating material or of other layers or structures on the substrate. Due to the precise control of the process gas in an RTP apparatus, the present invention also offers the possibility of carrying out selective reactions while curing the coating material. Exemplary selective reactions include oxidation or reduction processes occurring at certain layers or films, or parts thereof, on the substrate. When selective reactions are carried out, the process atmosphere can include an oxygen containing component and a hydrogen containing component e. The coated substrate may also be processed in a vacuum.

Chapter 3 : Rapid Thermal Oxidation

The RTP covered the latest developments in RTP and other short-time processing continuously aiming to point out the future direction in the Silicon ULSI devices and II-VI, III-V compound semiconductor devices.

A method for coating a surface of a substrate with a layer of a low dielectric constant material, comprising the steps of: The method of claim 1, wherein the coating material contains a solvent or a dispersant. The method of claim 2, further comprising the step of: The method of claim 1, wherein the curing step b is performed in an inert gas environment. The method of claim 4, wherein the curing step b is performed in an environment composed substantially of nitrogen. The method of claim 1, wherein the curing step b is performed in an environment in which the oxygen concentration is kept below about 10 ppm. The method of claim 1, wherein all steps are performed in an environment in which the oxygen concentration is kept below about 10 ppm. The method of claim 7, wherein all steps are performed in an environment composed substantially of nitrogen. The method of claim 1, wherein the coated substrate is held at the elevated temperature for a first time interval sufficient to at least partly convert the coating material to a low dielectric constant material. The method of claim 12, wherein the first time interval is 60 seconds or less. The method of claim 12, wherein the first time interval is 30 seconds or less. The method of claim 12, wherein the first time interval is 1 second or less. The method of claim 1, wherein the substrate is held within a single apparatus during the applying step a , the curing step b , and the cooling step c. The method of claim 1, wherein the substrate is held within a single apparatus during the curing step b and the cooling step c. The method of claim 16, wherein the substrate remains on a single holder. The method of claim 17, wherein the substrate remains on a single holder. The method of claim 1, wherein heating is by electromagnetic radiation generated by tungsten-halogen lamps, IR lamps, UV lamps, flash lamps or arc lamps or a combination of such lamps, by laser or by electrical heating means of an RIRTP system. The method of claim 1, wherein the layer of coating material is applied to the substrate by spin coating, spray coating, PVD or CVD. The method of claim 1, wherein the substrate is a semiconductor wafer. The method of claim 22, wherein the semiconductor wafer is formed from a single crystal silicon or polycrystalline silicon. The method of claim 22, wherein the semiconductor wafer has at least one active device region formed therein or thereon. The method of claim 24, wherein the semiconductor wafer further comprises a plurality of copper interconnect lines separated from an interlayer dielectric layer by a refractory barrier layer formed from a material selected from the group consisting of tantalum, tantalum nitride, titanium, titanium nitride, tungsten and tungsten nitride. The method of claim 12, wherein the coating material is cured for a first time interval sufficient to convert the coating material to a material with a low dielectric constant of below about 3. A method for curing a coating of a low dielectric constant material that has been applied to the surface of a substrate, comprising the steps of: The method of claim 28, further comprising: The method of claim 28, wherein the substrate is a semiconductor wafer. The method of claim 28, wherein the coating material is fully cured prior to the cooling step c. The method of claim 29, wherein the coating material is only partly cured prior to the spike heating step d. A semiconductor wafer coated with a low dielectric constant material that has been cured according to the method of claim Field of the Invention This invention relates to the formation of low dielectric constant "low k" layers suitable for use in semiconductor devices, and more particularly, to a method for curing low k dielectric materials using very short, relatively high temperature cycles. Background of the Invention Semiconductor chips are used in many applications, including as processor chips for computers, as integrated circuits, and as flash memory for hand held computing devices, wireless telephones, and digital cameras. Regardless of the application, ideally a semiconductor chip holds as many circuits or memory cells as possible per unit area. In this way, the size, weight, and energy consumption of devices that use semiconductor chips are minimized, while nevertheless improving the memory capacity and computing power of the devices. The escalating requirements for high density and performance associated with ultra-large scale integration semiconductor devices necessitate design

features of 0. A common circuit component of semiconductor chips is the transistor. In ultra-large-scale integrated ULSI semiconductor chips, a transistor is established by forming a polysilicon gate on a silicon substrate, and then forming a source region and a drain region side by side in the substrate beneath the gate by implanting appropriate dopant materials into the areas of the substrate that are to become the source and drain regions. The gate is insulated from the source and drain regions by a thin gate oxide layer. This generally-described structure cooperates to function as a transistor. A conventional method for forming patterned metal layers comprises a subtractive etching or etch back step as the primary metal forming technique. A metal layer is deposited on the first dielectric layer and patterned using photolithographic masking and etching techniques to form a desired conductive pattern comprising a metal feature separated by gaps, such as a plurality of metal lines with inter-wiring spacings therebetween. A dielectric layer is then applied to the resulting conductive pattern to fill in the gaps. The surface thereof is then planarized by conventional etching or chemical-mechanical polishing CMP techniques. A through-hole is then formed in the dielectric layer to expose a selected portion of an underlying metal feature. The exposed portion of the metal feature at the bottom of the through-hole serves as a contact pad. Upon filling the through-hole with conductive material, such as a metal plug, to form a conductive via, the bottom surface of the conductive via is in electrical contact with the underlying metal feature. Many ultra large scale integration ULSI devices presently manufactured are very complex and require multiple levels of metallization for interconnections. It has been common to repeat the above-described via formation process multiple times, e. As semiconductor devices become smaller, and on-chip device density correspondingly increases, signal delays due to capacitive coupling and crosstalk between closely spaced metal lines are increasing. These problems are exacerbated by the need to keep conductor lines as short as possible in order to minimize transmission delays, thus requiring multi-level wiring schemes for the chip. As a consequence, capacitive coupling between conductive lines significantly limits circuit speed. A problem encountered in highly miniaturized semiconductor devices employing multiple metallization levels and reduced inter-wiring spacings in both the horizontal and vertical dimensions is related to the resistance-capacitance RC time constant of the system. If intra-metal capacitance is high, electrical inefficiencies and inaccuracies increase. It has been recognized that a reduction in capacitance within the multi-level metallization system will reduce the RC time constant between the conductive lines. The dielectric constant is based on a scale where 1. As used herein, the term "low k" will refer to materials that have dielectric constants less than 3. The drive to reduce the RC delay associated with the metal interconnect lines also has led the industry to move away from the traditional aluminum Al interconnect metal lines in favor of copper Cu based metallization. The sheet resistivity of copper-based metal lines can be half that of aluminum-based metal systems. However, copper diffuses more easily into the inter-level dielectric at normal processing temperatures, thereby degrading the dielectric and weakening the isolation between adjacent metal lines. If the copper diffuses into the underlying silicon, then the device performance also will be degraded. To prevent unwanted diffusion, most copper processes e. For very narrow copper lines, applying an appropriate refractory barrier metal layer is very important. Thick barrier layers can result in higher metal line resistance than found in Al lines. Therefore, the thickness of the barrier layer must be minimized. The drive towards increased miniaturization and the resultant increase in the RC time constant also have served as an impetus for the development of newer, low dielectric constant "low k" materials as substitutes for conventional higher dielectric constant silicon oxide-based ILD materials. The ILD films or layers must normally be formed at relatively low temperatures in order to avoid damage to or destruction of underlying conductors. Lower processing temperatures can increase the time needed for layer formation leading to decreased manufacturing throughput. One prior process for applying low k materials to semiconductor substrates is shown in U. First, a layer of low k material resin combined with a solvent or dispersant therefor is applied to a substrate by a spin coating process. The method shown in U. Temperature ramp up and ramp down of the coated substrate is controlled by regulating the spacing between the hot plates and the substrate, and controlling the length of time the substrate is held at a certain spacing. For baking,

curing and cooling the coated substrate, three hot plates of different temperatures are used. The substrate is processed sequentially by being transferred between the hot plates. In view of this transporting, the heating of the substrate is not controlled as precisely and rapidly as is desirable for substrates that include copper interconnects. See EP 0 A2. Such typical furnace curing processes place severe demands on process integration. Long cure times result in decreased manufacturing throughput. However, increasing cure temperatures to reduce cure times can cause damage to, or even destroy, underlying conductors. In addition, it is difficult to suppress copper diffusion for a long duration cure, even when the cure is carried out at a lower temperature. Nevertheless, higher curing temperatures can also lead to increased copper diffusion rates. Other deficiencies of the current processes include inadequate control of the thermal budget. Although the curing is described as rapid, the curing times used are up to ten minutes, which is long enough to cause undesirable diffusion of metal interconnects sought to be avoided. The processing described would be particularly undesirable for copper interconnects. See also related U. Thus, there exists a need for a method of forming a layer of low dielectric constant material on a surface of a substrate characterized by shorter curing times, higher curing temperatures, and precise control of thermal budget without the requirement of a thicker refractory barrier metal layers. The coated substrate is held at the elevated temperature for a first time interval sufficient to convert the coating material to a low dielectric constant material of high thermal stability. The purpose of curing step b is mainly to initiate the chemical reaction s that produce films with high thermal stability. For most films, step b has very little or no effect on the dielectric constant, meaning that the k value remains nearly unaffected after the cure. Before curing, a pre-heating or baking step can be carried out to evaporate any solvents remaining in the coating material. Preferably, the baking step temperature is lower than the elevated temperature. The first time interval of curing step b is generally shorter than that used in prior art methods. Depending upon the low dielectric constant material low k material used, the temperature-time curve with which the substrate is processed, the gas atmosphere in which the substrate is processed, and the heating method, the first time interval is preferably less than 30 seconds, more preferably less than 25 seconds, and under certain conditions even less than 20 seconds. Preferably, the substrate is heated in a lamp-based RTP apparatus, wherein heating is by electromagnetic radiation, e. The electromagnetic radiation, or at least part of it, also can be generated by laser. Due to the high heating rate of the curing step, the first time interval for holding the coated substrate at an elevated temperature advantageously can be reduced. When heating is by UV radiation, the first time interval can be reduced to as short as 20 seconds. The present invention also can be carried out using "susceptor-based RTP" systems that do not employ lamps to achieve rapid heating rates. One example of such a "susceptor-based RTP" system is described in U. The wafer is rapidly inserted into a furnace cavity maintained at a substantially constant processing temperature, controllably heated by electrical heating means, preferably resistor heating means. Due to the rapid insertion, the wafer rapidly heats to the desired process temperature.

Chapter 4 : Rapid thermal processing RTP and rapid thermal annealing RTA

"The international symposium on Rapid Thermal and Other Short-Time Processing Technologies II was held from March 24 through March 29, in Washington DC as part of the th Meeting of the Electrochemical Society"--Preface.

High temperatures allow diffusion processes to occur fast. The time at the high temperature soaking time is long enough to allow the desired transformation to occur. Cooling is done slowly to avoid the distortion warping of the metal piece, or even cracking, caused by stresses induced by differential contraction due to thermal inhomogeneities. Benefits of annealing are: Reverting the effect of cold work by process annealing eases further deformation. Heating allows recovery and recrystallization but is usually limited to avoid excessive grain growth and oxidation. Full anneal involves taking hypoeutectoid alloys to the austenite phase and hypereutectoid alloys over the eutectoid temperature Fig. Spheroidizing consists in prolongued heating just below the eutectoid temperature, which results in the soft spheroidite structure discussed in Sect. This achieves maximum softness that minimizes the energy needed in subsequent forming operations. Heat Treatment of Steels 1. If the piece is thick, the interior may cool too slowly so that full martensitic conversion is not achieved. Thus, the martensitic content, and the hardness, will drop from a high value at the surface to a lower value in the interior of the piece. Hardenability is the ability of the material to be hardened by forming martensite. Hardenability is measured by the Jominy end-quench test Fig. Hardenability is then given as the dependence of hardness on distance from the quenched end. High hardenability means that the hardness curve is relatively flat. Cooling is fastest using water, then oil, and then air. Fast cooling brings the danger of warping and formation of cracks, since it is usually accompanied by large thermal gradients. The shape and size of the piece, together with the heat capacity and heat conductivity are important in determining the cooling rate for different parts of the metal piece. Heat capacity is the energy content of a heated mass, which needs to be removed for cooling. Heat conductivity measures how fast this energy is transported to the colder regions of the piece. Precipitation Hardening Hardening can be enhanced by extremely small precipitates that hinder dislocation motion. The precipitates form when the solubility limit is exceeded. Precipitation hardening is also called age hardening because it involves the hardening of the material over a prolonged time. If the process is continued for a very long time, eventually the hardness decreases. This is called overaging. The requirements for precipitation hardening are: It is accelerated at high temperatures. Hardening occurs because the deformation of the lattice around the precipitates hinder slip. Aging that occurs at room temperature is called natural aging, to distinguish from the artificial aging caused by premeditated heating.

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Chapter 5 : Chapter Thermal Processing of Metal Alloys

Abstract. Rapid thermal annealing (RTA) with a short dwell time at maximum temperature is used with ion implantation to form shallow junctions and polycrystalline-Si gate electrodes in complementary, metal-oxide semiconductor (CMOS) Si processing.

A method for coating a surface of a semiconductor substrate with a layer of a low dielectric constant material, having a dielectric constant of less than 3. The method of claim 1, wherein the coating material contains a solvent or a dispersant. The method of claim 1 or 2, further comprising the step of: The method of any one of the preceding claims, wherein the curing step b is performed in an inert gas environment. The method of claim 4, wherein the curing step b is performed in an environment composed substantially of nitrogen. The method of any one of the preceding claims, wherein the curing step b is performed in an environment in which the oxygen concentration is kept below about 10 ppm. The method of any one of the preceding claims, wherein all steps are performed in an environment in which the oxygen concentration is kept below about 10 ppm. The method of claim 7, wherein all steps are performed in an environment composed substantially of nitrogen. The method of any one of the preceding claims, wherein the coated substrate is held at the elevated temperature for a first time interval sufficient to at least partly convert the coating material to a low dielectric constant material. The method of claim 12, wherein the first time interval is 60 seconds or less. The method of claim 12, wherein the first time interval is 30 seconds or less. The method of claim 12, wherein the first time interval is 1 second or less. The method of any one of the preceding claims, wherein the substrate is held within a single apparatus during the applying step a , the curing step b , and the cooling step c. The method of any one of the preceding claims, wherein the substrate is held within a single apparatus during the curing step b and the cooling step c. The method of claim 16 or 17, wherein the substrate remains on a single holder. The method of any one of the preceding claims, wherein heating is by electromagnetic radiation generated by tungsten-halogen lamps, IR lamps, UV lamps, flash lamps or arc lamps or a combination of such lamps, by laser or by electrical heating means of an RIRTP system. The method of any one of the preceding claims, wherein the layer of coating material is applied to the substrate by spin coating, spray coating, PVD or CVD. The method of any one of the preceding claims, wherein the semiconductor wafer is formed from a single crystal silicon or polycrystalline silicon. The method of any one of the preceding claims, wherein the semiconductor wafer has at least one active device region formed therein or thereon. The method of claim 22, wherein the semiconductor wafer further comprises a plurality of copper interconnect lines separated from an interlayer dielectric layer by a refractory barrier layer formed from a material selected from the group consisting of tantalum, tantalum nitride, titanium, titanium nitride, tungsten and tungsten nitride. The method of claim 12, wherein the coating material is cured for a first time interval sufficient to convert the coating material to said material having said low dielectric constant below 3. The method of claim 12, wherein the coating material is cured for a first time interval sufficient to convert the coating material to a material with a low dielectric constant of below about 3. The method of claim 26, further comprising: The method of claim 26, wherein the coating material is fully cured prior to the cooling step c. The method of claim 27, wherein the coating material is only partly cured prior to the spike heating step d. Field of the Invention This invention relates to the formation of low dielectric constant "low k" layers suitable for use in semiconductor devices, and more particularly, to a method for curing low k dielectric materials using very short, relatively high temperature cycles. Background of the Invention Semiconductor chips are used in many applications, including as processor chips for computers, as integrated circuits, and as flash memory for hand held computing devices, wireless telephones, and digital cameras. Regardless of the application, ideally a semiconductor chip holds as many circuits or memory cells as possible per unit area. In this way, the size, weight, and energy consumption of devices that use semiconductor chips are minimized, while nevertheless improving the memory capacity and computing power of the devices. The escalating requirements for high

density and performance associated with ultra-large scale integration semiconductor devices necessitate design features of 0. A common circuit component of semiconductor chips is the transistor. In ultra-large-scale integrated ULSI semiconductor chips, a transistor is established by forming a polysilicon gate on a silicon substrate, and then forming a source region and a drain region side by side in the substrate beneath the gate by implanting appropriate dopant materials into the areas of the substrate that are to become the source and drain regions. The gate is insulated from the source and drain regions by a thin gate oxide layer. This generally-described structure cooperates to function as a transistor. A conventional method for forming patterned metal layers comprises a subtractive etching or etch back step as the primary metal forming technique. A metal layer is deposited on the first dielectric layer and patterned using photolithographic masking and etching techniques to form a desired conductive pattern comprising a metal feature separated by gaps, such as a plurality of metal lines with inter-wiring spacings therebetween. A dielectric layer is then applied to the resulting conductive pattern to fill in the gaps. The surface thereof is then planarized by conventional etching or chemical-mechanical polishing CMP techniques. A through-hole is then formed in the dielectric layer to expose a selected portion of an underlying metal feature. The exposed portion of the metal feature at the bottom of the through-hole serves as a contact pad. Upon filling the through-hole with conductive material, such as a metal plug, to form a conductive via, the bottom surface of the conductive via is in electrical contact with the underlying metal feature. Many ultra large scale integration ULSI devices presently manufactured are very complex and require multiple levels of metallization for interconnections. It has been common to repeat the above-described via formation process multiple times, e. As semiconductor devices become smaller, and on-chip device density correspondingly increases, signal delays due to capacitive coupling and crosstalk between closely spaced metal lines are increasing. These problems are exacerbated by the need to keep conductor lines as short as possible in order to minimize transmission delays, thus requiring multi-level wiring schemes for the chip. As a consequence, capacitive coupling between conductive lines significantly limits circuit speed. A problem encountered in highly miniaturized semiconductor devices employing multiple metallization levels and reduced inter-wiring spacings in both the horizontal and vertical dimensions is related to the resistance-capacitance RC time constant of the system. If intra-metal capacitance is high, electrical inefficiencies and inaccuracies increase. It has been recognized that a reduction in capacitance within the multi-level metallization system will reduce the RC time constant between the conductive lines. The dielectric constant is based on a scale where 1. As used herein, the term "low k" will refer to materials that have dielectric constants less than 3. The drive to reduce the RC delay associated with the metal interconnect lines also has led the industry to move away from the traditional aluminum Al interconnect metal lines in favor of copper Cu based metallization. The sheet resistivity of copper-based metal lines can be half that of aluminum-based metal systems. However, copper diffuses more easily into the inter-level dielectric at normal processing temperatures, thereby degrading the dielectric and weakening the isolation between adjacent metal lines. If the copper diffuses into the underlying silicon, then the device performance also will be degraded. To prevent unwanted diffusion, most copper processes e. For very narrow copper lines, applying an appropriate refractory barrier metal layer is very important. Thick barrier layers can result in higher metal line resistance than found in Al lines. Therefore, the thickness of the barrier layer must be minimized. The drive towards increased miniaturization and the resultant increase in the RC time constant also have served as an impetus for the development of newer, low dielectric constant "low k" materials as substitutes for conventional higher dielectric constant silicon oxide-based ILD materials. The ILD films or layers must normally be formed at relatively low temperatures in order to avoid damage to or destruction of underlying conductors. Lower processing temperatures can increase the time needed for layer formation leading to decreased manufacturing throughput. One prior process for applying low k materials to semiconductor substrates is shown in U. First, a layer of low k material resin combined with a solvent or dispersant therefor is applied to a substrate by a spin coating process. The method shown in U. Temperature ramp up and ramp down of the coated substrate is controlled by regulating the spacing between the hot plates and the substrate, and controlling the length of

time the substrate is held at a certain spacing. For baking, curing and cooling the coated substrate, three hot plates of different temperatures are used. The substrate is processed sequentially by being transferred between the hot plates. In view of this transporting, the heating of the substrate is not controlled as precisely and rapidly as is desirable for substrates that include copper interconnects. See EP 0 A2. Such typical furnace curing processes place severe demands on process integration. Long cure times result in decreased manufacturing throughput. However, increasing cure temperatures to reduce cure times can cause damage to, or even destroy, underlying conductors. In addition, it is difficult to suppress copper diffusion for a long duration cure, even when the cure is carried out at a lower temperature. Nevertheless, higher curing temperatures can also lead to increased copper diffusion rates. Other deficiencies of the current processes include inadequate control of the thermal budget. Although the curing is described as rapid, the curing times used are up to ten minutes, which is long enough to cause undesirable diffusion of metal interconnects sought to be avoided. The processing described would be particularly undesirable for copper interconnects. See also related U. Thus, there exists a need for a method of forming a layer of low dielectric constant material on a surface of a substrate characterized by shorter curing times, higher curing temperatures, and precise control of thermal budget without the requirement of a thicker refractory barrier metal layers. The coated substrate is held at the elevated temperature for a first time interval sufficient to convert the coating material to a low dielectric constant material of high thermal stability. The purpose of curing step b is mainly to initiate the chemical reaction s that produce films with high thermal stability. For most films, step b has very little or no effect on the dielectric constant, meaning that the k value remains nearly unaffected after the cure. Before curing, a pre-heating or baking step can be carried out to evaporate any solvents remaining in the coating material. Preferably, the baking step temperature is lower than the elevated temperature. The first time interval of curing step b is generally shorter than that used in prior art methods. Depending upon the low dielectric constant material low k material used, the temperature-time curve with which the substrate is processed, the gas atmosphere in which the substrate is processed, and the heating method, the first time interval is preferably less than 30 seconds, more preferably less than 25 seconds, and under certain conditions even less than 20 seconds. Preferably, the substrate is heated in a lamp-based RTP apparatus, wherein heating is by electromagnetic radiation, e. The electromagnetic radiation, or at least part of it, also can be generated by laser. Due to the high heating rate of the curing step, the first time interval for holding the coated substrate at an elevated temperature advantageously can be reduced. When heating is by UV radiation, the first time interval can be reduced to as short as 20 seconds. The present invention also can be carried out using "susceptor-based RTP" systems that do not employ lamps to achieve rapid heating rates. One example of such a "susceptor-based RTP" system is described in U. The wafer is rapidly inserted into a furnace cavity maintained at a substantially constant processing temperature, controllably heated by electrical heating means, preferably resistor heating means. Due to the rapid insertion, the wafer rapidly heats to the desired process temperature. The first time interval of curing step b is sufficient to at least partially convert the coated material into a thermally stable low k material film. If the coated substrate is heated only once to the elevated temperature, without stepped intervals, the first time interval is selected such that within this time the material is fully converted. In spiking processes, the first time interval may be less than one second, depending upon the heating apparatus used. In spiking processes according to this invention, the first time interval of curing step b is determined by the change from heating to cooling, and can even be reduced to below one second, such as about 0.

Chapter 6 : Thermal oxidation - Wikipedia

Low thermal budgets can be achieved by either operating at a low temperature, and hence low D, as during molecular beam epitaxy (MBE) (Bean, ; Iyer et al.,) or ultra high vacuum chemical vapor deposition (UHVCVD) (Meyerson,), or by operating at a high temperature for a very short time, as during rapid thermal processing chemical.

Pasteurization Thermal processing implies the controlled use of heat to increase, or reduce depending on circumstances, the rates of reactions in foods. A common example is the retorting of canned foods to effect sterilization. The object of sterilization is to destroy all microorganisms, that is, bacteria, yeasts and moulds, in the food material to prevent decomposition of the food, which makes it unattractive or inedible. Also, sterilization prevents any pathogenic disease-producing organisms from surviving and being eaten with the food. Pathogenic toxins may be produced during storage of the food if certain organisms are still viable. Microorganisms are destroyed by heat, but the amount of heating required for the killing of different organisms varies. Also, many bacteria can exist in two forms, the vegetative or growing form and the spore or dormant form. The spores are much harder to destroy by heat treatment than are the vegetative forms. Studies of the microorganisms that occur in foods, have led to the selection of certain types of bacteria as indicator organisms. These are the most difficult to kill, in their spore forms, of the types of bacteria which are likely to be troublesome in foods. A frequently used indicator organism is Clostridium botulinum. This particular organism is a very important food poisoning organism as it produces a deadly toxin and also its spores are amongst the most heat resistant. Processes for the heat treatment of foodstuffs are therefore examined with respect to the effect they would have on the spores of C. If the heat process would not destroy this organism then it is not adequate. Thermal Death Time It has been found that microorganisms, including C. At any given temperature, the spores are killed at different times, some spores being apparently more resistant to heat than other spores. If a graph is drawn, the number of surviving spores against time of holding at any chosen temperature, it is found experimentally that the number of surviving spores fall asymptotically to zero. Methods of handling process kinetics are well developed and if the standard methods are applied to such results, it is found that thermal death of microorganisms follows, for practical purposes, what is called a first-order process at a constant temperature see for example Earle and Earle, This implies that the fractional destruction in any fixed time interval, is constant. It is thus not possible, in theory at least, to take the time when all of the organisms are actually destroyed. Instead it is practicable, and very useful, to consider the time needed for a particular fraction of the organisms to be killed. The rates of destruction can in this way be related to: Of course the surviving number must be small indeed, very much less than one, to ensure adequate safety. However, this concept, which includes the admissibility of survival numbers of much less than one per container, has been found to be very useful. From such considerations, the ratio of the initial to the final number of surviving organisms becomes the criterion that determines adequate treatment. A combination of historical reasons and extensive practical experience has led to this number being set, for C. For other organisms, and under other circumstances, it may well be different. The results of experiments to determine the times needed to reduce actual spore counts from to 1 the lower, open, circles or to 0 the upper, closed, circles are shown in Fig. Thermal death time curve for Clostridium botulinum Based on research results from the American Can Company In this graph, these times are plotted against the different temperatures and it shows that when the logarithms of these times are plotted against temperatures, the resulting graph is a straight line. The mean times on this graph are called thermal death times for the corresponding temperatures. Note that these thermal death times do not represent complete sterilization, but a mathematical concept which can be considered as effective sterilization, which is in fact a survival ratio of 1: This is done by combining the thermal death time data with the time-temperature relationships at the point in the can that heats slowest. Generally, this point is on the axis of the can and somewhere close to the geometric centre. Using either the unsteady-state heating curves or experimental measurements with a thermocouple at the slowest heating point

in a can, the temperature-time graph for the can under the chosen conditions can be plotted. This curve has then to be evaluated in terms of its effectiveness in destroying C. In this way the engineering data, which provides the temperatures within the container as the process is carried out, are combined with kinetic data to evaluate the effect of processing on the product. In our example, reading from Fig. If the total F value so found is below 2. Experimentally, it has been found that if the logarithm of t, the thermal death time, is plotted against the temperature, a straight-line relationship is obtained. This is shown in Fig.

Chapter 7 : Rapid Thermal and Other Short-Time Processing Technologies III : P. Timans :

Proceedings, the th ECS Meetings, Symposium on Rapid Thermal and Other Short-Time Processing Technologies III, Washington, DC, March PHYSICAL CHARACTERIZATION OF ZrO2 FILMS ON SILICON.

Once the coating material has been converted to a low dielectric constant material with desired properties, the coated substrate is cooled. Alternatively, spike heating raises and promptly lowers the temperature of the coated substrate to effect curing in one or a series of spike heating steps. The method allows for a thinner refractory barrier metal layer thickness to prevent copper diffusion, and uses shorter curing times resulting in higher throughput. Background of the Invention Semiconductor chips are used in many applications, including as processor chips for computers, as integrated circuits, and as flash memory for hand held computing devices, wireless telephones, and digital cameras. Regardless of the application, ideally a semiconductor chip holds as many circuits or memory cells as possible per unit area. In this way, the size, weight, and energy consumption of devices that use semiconductor chips are minimized, while nevertheless improving the memory capacity and computing power of the devices. The escalating requirements for high density and performance associated with ultra-large scale integration semiconductor devices necessitate design features of 0. A common circuit component of semiconductor chips is the transistor. In ultra-large-scale integrated ULSI semiconductor chips, a transistor is established by forming a polysilicon gate on a silicon substrate, and then forming a source region and a drain region side by side in the substrate beneath the gate by implanting appropriate dopant materials into the areas of the substrate that are to become the source and drain regions. The gate is insulated from the source and drain regions by a thin gate oxide layer. This generally-described structure cooperates to function as a transistor. A conventional method for forming patterned metal layers comprises a subtractive etching or etch back step as the primary metal forming technique. A metal layer is deposited on the first dielectric layer and patterned using photolithographic masking and etching techniques to form a desired conductive pattern comprising a metal feature separated by gaps, such as a plurality of metal lines with inter-wiring spacings therebetween. A dielectric layer is then applied to the resulting conductive pattern to fill in the gaps. The surface thereof is then planarized by conventional etching or chemical-mechanical polishing CMP techniques. A through-hole is then formed in the dielectric layer to expose a selected portion of an underlying metal feature. The exposed portion of the metal feature at the bottom of the through-hole serves as a contact pad. Upon filling the through-hole with conductive material, such as a metal plug, to form a conductive via, the bottom surface of the conductive via is in electrical contact with the underlying metal feature. Many ultra large scale integration ULSI devices presently manufactured are very complex and require multiple levels of metallization for interconnections. It has been common to repeat the above-described via formation process multiple times, e. As semiconductor devices become smaller, and on-chip device density correspondingly increases, signal delays due to capacitive coupling and crosstalk between closely spaced metal lines are increasing. These problems are exacerbated by the need to keep conductor lines as short as possible in order to minimize transmission delays, thus requiring multi-level wiring schemes for the chip. As a consequence, capacitive coupling between conductive lines significantly limits circuit speed. A problem encountered in highly miniaturized semiconductor devices employing multiple metallization levels and reduced inter-wiring spacings in both the horizontal and vertical dimensions is related to the resistance-capacitance RC time constant of the system. If intra-metal capacitance is high, electrical inefficiencies and inaccuracies increase. It has been recognized that a reduction in capacitance within the multi-level metallization system will reduce the RC time constant between the conductive lines. The dielectric constant is based on a scale where 1. The drive to reduce the RC delay associated with the metal interconnect lines also has led the industry to move away from the traditional aluminum Al interconnect metal lines in favor of copper Cu based metallization. The sheet resistivity of copper-based metal lines can be half that of aluminum-based metal systems. However, copper diffuses more easily into the inter-level dielectric at normal

processing temperatures, thereby degrading the dielectric and weakening the isolation between adjacent metal lines. If the copper diffuses into the underlying silicon, then the device performance also will be degraded. To prevent unwanted diffusion, most copper processes e. For very narrow copper lines, applying an appropriate refractory barrier metal layer is very important. Thick barrier layers can result in higher metal line resistance than found in Al lines. Therefore, the thickness of the barrier layer must be minimized. The ILD films or layers must normally be formed at relatively low temperatures in order to avoid damage to or destruction of underlying conductors. Lower processing temperatures can increase the time needed for layer formation leading to decreased manufacturing throughput. One prior process for applying low k materials to semiconductor substrates is shown in U. First, a layer of low k material resin combined with a solvent or dispersant therefor is applied to a substrate by a spin coating process. The method shown in U. Temperature ramp up and ramp down of the coated substrate is controlled by regulating the spacing between the hot plates and the substrate, and controlling the length of time the substrate is held at a certain spacing. For baking, curing and cooling the coated substrate, three hot plates of different temperatures are used. The substrate is processed sequentially by being transferred between the hot plates. In view of this transporting, the heating of the substrate is not controlled as precisely and rapidly as is desirable for substrates that include copper interconnects. See EP 0 A2. Such typical furnace curing processes place severe demands on process integration. Long cure times result in decreased manufacturing throughput. However, increasing cure temperatures to reduce cure times can cause damage to, or even destroy, underlying conductors. In addition, it is difficult to suppress copper diffusion for a long duration cure, even when the cure is carried out at a lower temperature. Nevertheless, higher curing temperatures can also lead to increased copper diffusion rates. Other deficiencies of the current processes include inadequate control of the thermal budget. Although the curing is described as rapid, the curing times used are up to ten minutes, which is long enough to cause undesirable diffusion of metal interconnects sought to be avoided. The processing described would be particularly undesirable for copper interconnects. See also related U. Thus, there exists a need for a method of forming a layer of low dielectric constant material on a surface of a substrate characterized by shorter curing times, higher curing temperatures, and precise control of thermal budget without the requirement of a thicker refractory barrier metal layers. The coated substrate is held at the elevated temperature for a first time interval sufficient to convert the coating material to a low dielectric constant material of high thermal stability. The purpose of curing step b is mainly to initiate the chemical reaction s that produce films with high thermal stability. For most films, step b has very little or no effect on the dielectric constant, meaning that the k value remains nearly unaffected after the cure. Before curing, a pre-heating or baking step can be carried out to evaporate any solvents remaining in the coating material. Preferably, the baking step temperature is lower than the elevated temperature. The first time interval of curing step b is generally shorter than that used in prior art methods. Depending upon the low dielectric constant material low k material used, the temperature-time curve with which the substrate is processed, the gas atmosphere in which the substrate is processed, and the heating method, the first time interval is preferably less than 30 seconds, more preferably less than 25 seconds, and under certain conditions even less than 20 seconds. Preferably, the substrate is heated in a lamp-based RTP apparatus, wherein heating is by electromagnetic radiation, e. The electromagnetic radiation, or at least part of it, also can be generated by laser. Due to the high heating rate of the curing step, the first time interval for holding the coated substrate at an elevated temperature advantageously can be reduced. When heating is by UV radiation, the first time interval can be reduced to as short as 20 seconds. The wafer is rapidly inserted into a furnace cavity maintained at a substantially constant processing temperature, controllably heated by electrical heating means, preferably resistor heating means. Due to the rapid insertion, the wafer rapidly heats to the desired process temperature. The first time interval of curing step b is sufficient to at least partially convert the coated material into a thermally stable low k material film. If the coated substrate is heated only once to the elevated temperature, without stepped intervals, the first time interval is selected such that within this time the material is fully converted. In spiking processes, the first time interval may be less than one

second, depending upon the heating apparatus used. In spiking processes according to this invention, the first time interval of curing step b is determined by the change from heating to cooling, and can even be reduced to below one second, such as about 0. The present invention also embraces temperature-time processes in which the coated substrate is heated to various elevated temperatures in a sequence of time intervals. The time intervals can comprise intervals in which the substrate is cooled down to lower temperatures. Multiple spike processing, in which one spike is followed by at least one other spike, may be used. The time interval between two spike processes, meaning the time interval between subsequent rapid cooling and rapid heating, is preferably less than about 30 seconds, and can be as short as about 0. In multiple spike processes, it can be sufficient for the coating material to be only partially converted into low k material within one spike process or within one time interval in which the substrate is heated to an elevated temperature because the coated material will be fully converted in a following time interval or spike process in the sequence. An elevated temperature is selected within a temperature range embracing the lowest temperature at which curing of the coating material starts at the chosen process parameters and the highest temperature at which the coating material starts to decompose. Process parameters that may impact the chosen elevated temperature range include atmosphere content and pressure, coating material composition, heating rate, and spectrum of electromagnetic radiation selected for heating. Ideally, the highest temperature in the temperature range is lower than the decomposition temperature of the coating material to account for the possibility that the heating will not be uniform across the substrate. This will ensure that the low k material does not decompose even if the temperature distribution across the substrate is not uniform. Preferably, the curing time interval is 60 seconds or less, most preferably about 30 seconds. Preferably, the gas atmosphere in which the coated substrate is processed is dominated by an inert gas. Depending upon the temperature, molecular nitrogen can be used as the inert gas. However, noble gases argon and helium or noble gases mixed with nitrogen can be used. As one possibility, with the beginning of the temperature ramp down, the composition of the atmosphere can be changed by adding helium to the nitrogen gas. The thermal conductivity can be increased by adding helium, which helps to speed the cooling rate. If the coating or low k material does not react with molecular hydrogen gas, such gas also can be introduced to manipulate the thermal conductivity of the process atmosphere. In addition, added hydrogen gas or ammonia can prevent oxidation of the coating material or of other layers or structures on the substrate. Due to the precise control of the process gas in an RTP apparatus, the present invention also offers the possibility of carrying out selective reactions while curing the coating material. Exemplary selective reactions include oxidation or reduction processes occurring at certain layers or films, or parts thereof, on the substrate. When selective reactions are carried out, the process atmosphere can include an oxygen containing component and a hydrogen containing component e. The coated substrate may also be processed in a vacuum. The coated substrate also may be processed in a vacuum. In the preferred embodiment, the curing step is performed in an environment composed substantially of nitrogen. Most preferably, the oxygen concentration in the curing environment is maintained below about 10 ppm. In addition, the method may also include the step of preheating or baking the coated substrate to a first temperature prior to curing so as to liberate substantially all of any added solvent or dispersant from the coating material. First, the inventive method obtains equivalent curing in a shorter time. Shorter curing times result in higher throughput.